The usual bugs and errors have begun to show up. Here are corrections so far reported...

The positions of C4 and C5, (The VCO Colpitts Oscillator feedback capacitors) are shown reversed on the PCB layout. The circuit diagram and table in Appendix 1 are correct.

No values are supplied for R9 / C16, the auxiliary filter in the PLL. These should be chosen so their 3dB cutoff frequency is more than 4 times the PLL bandwidth. For the 144MHz example given, the PLL bandwidth is of the order of 1000Hz, so a cutoff of 4kHz is needed. Values of 1k and 33nF respectively are suitable here for a cutoff at 4.8kHz.

The PCB layout shows two capacitors in the C19 and C16 position with only C16 shown on the circuit diagram. The second position is there in case additional decoupling is needed. For example, a high value capacitor may be desired with a low loop bandwidth, and this could be inadequate for removing VHF leakage. In this event, add a 1nF at the C19 position and make C16 the large value PLL filter component.

R27 on the circuit diagram is R3 on the PCB layout.

There are two C13 capacitors shown on the circuit diagram, but only one on the PCB the 2.2uF one. The one on the circuit diagram labelled 100nF is in error.