Simple 1.9MHz Power Amplifier

G4JNT April 2009

This started out as a quick throw-together design to get a WSPR beacon running on 1840kHz without tying up the main shack rig. The signal is generated directly from a DDS/PIC/GPS combination http://www.g4jnt.com/WSPRBCNS.ZIP but after building it, I found it worked better than designed, to such an extent that something odd is happening that at some point needs further investigation

Notably :

It gives out considerably more power than it was designed for
Efficiency is appreciably better than may be expected for a class-C design.

Design Process :

I wanted a simple class-C PA to give about 10 Watts out, say 12 Watts to allow for O/P filter losses. It had to run from a nominal 13V supply and a low cost switching type Mosfet was the obvious choice for the PA. I had several IRF540 devices, which have a low on resistance (50m-ohms) and rated at 100V so should give a safe voltage margin. Current is rated at 33A max.

First the O/P matching network :

10 Watts from a 12V rail needs $R_L = 12^2 / (2 * 10) = 7.2\Omega$
With a 13V rail, P_{out} for this R_L will be around 12 Watts

Remembering back to the distant past where such PAs were commonplace, I recalled a Q of 5 to 6 was stated as being typical for solid-state tank circuits so an L-C-C network transforming 50Ω to 7.2Ω with this Q was derived. Values came out to be L = 3.6uH, C_{shunt} = 1220pF C_{series} = 700pF for use at 1840kHz

At R_L = 7Ω the DC supply choke needs to be of the order of 5 – 10 times this value, and for convenience I used the same value as the tank L – 3.6uH

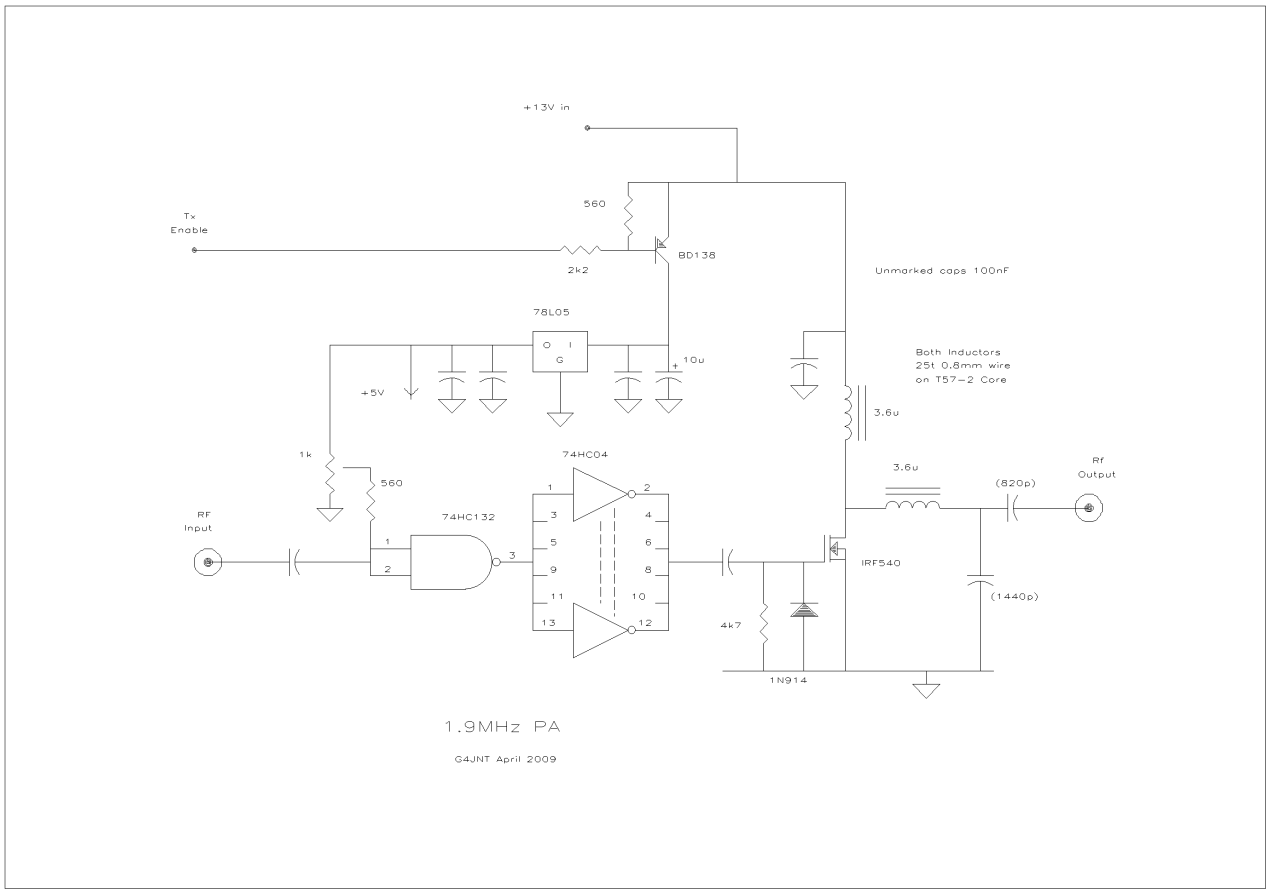
Drive Circuitry :

Drive was kept simple, with all six paralleled gates of a hex-inverter chip, driven by a Schmitt input buffer to make absolutely sure there could be no instability at zero drive level. According to the data sheet the IRF540 would switch quite happily at 5V – certainly so at the modest current it is running at here. A preset was added at the input to allow optimum setting of input bias for minimum drive level, and might offer the opportunity to alter the drive duty cycle.

The drive to the FET was taken through a DC restoration capacitor / diode to ensure that if the HC04 chip should sit at a logic ‘1’, the device wouldn’t be turned hard on, shorting the power supply.

Breadboard :

A breadboard was put together as shown below (also at http://www.g4jnt.com/ClassCPA.gif)



On testing a few big surprises came to light. The PA worked best at a frequency appreciably higher than it was designed for, giving maximum power at around 2MHz rather than 1.84MHz. In fact at 1.84MHz the output was rather messy, with some spurious / instability present. At 2MHz it was giving a very clean output and the power being supplied to the load was over 30 Watts !

Also, the device was running rather cooler that I might have expected, so measured the DC-RF conversion efficiency. Slightly more than 75%

Probing the voltage waveforms showed that the output of the 74HC132 buffer was very close to a squarewave as intended, but the output of the HC04 devices, and the waveform on the FET gate had an extended duty-cycle, of about 70% - in other words it was being kept turned on even after the drive had fallen away.

The waveform at the drain of the FET was the biggest surprise. It consisted of a more-or-less square topped spike of 100 Volts for about 20% of the RF cycles, falling back to close to zero until the device turned on properly at the 50% point where drain volts really went to zero. It is presumably this spike, being fed back through the drain-gate capacitance and

adding to the end of the drive on-period that is giving the unexpected high duty cycle gate / drive waveform.

Now, as we have a 20% duty cycle 100V spike hitting the L-C-C combination, this presumably accounts for the higher than expected output power.

Practical end-product:

As I wanted a PA for transmitting with, and had better things to do than spend ages trying to understand just how exactly this thing was working, I scaled the C values in the matching network from 2 to 1.84MHz, tested it at this frequency (worked fine, 30 Watts, clean). Added a 5^{th} order 2.1MHz elliptic filter ([1]) and put it on air. P_{out} was now a little over 25 Watts. The new capacitor values are those shown in the circuit diagram.

Explanations & queries :

- The 100V spike is exactly as would be seen in a flyback topology Switch Mode PSU.

- but with a 3.6uH inductor, a V_{on} duration of 0.6us would only allow a peak current of 1.7A to build up. So continuous mode has to be assumed (in flyback topology ?)

- With a non-sinusoidal drive the output matching network presents a higher impedance at harmonics.

- Efficiency is better that the traditionally quoted 66 – 70% of a class C design, so is this more like class D / E / F …..Z or whatever!

- Both output inductors were running quite hot, in fact they were the hottest components altogether and could have been dissipating a watt or two each Bigger cores would probably give even higher efficiency.

[1] The Low Pass Filter was already built and had been designed for high power use, originally for the GB3SSS beacon at Poldhu.