ICS-501 PLL Multiplier Chip Phase Noise Plots

G4JNT Nov 2012

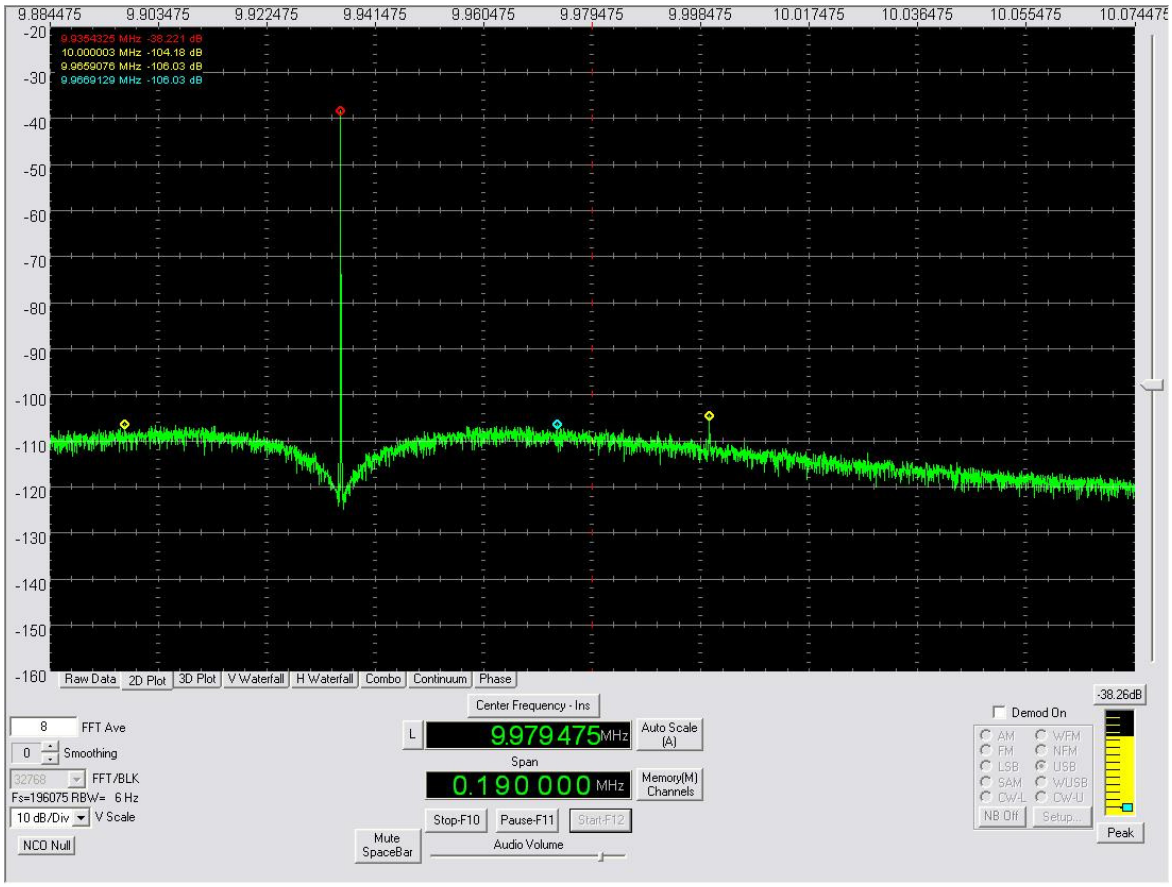
The internal oscillator of the ICS-501 was used with two crystals, at nominally 20.099MHz and 12MHz. The output for all plots, apart from the 24MHz output, were obtained by mixing down with a 116MHz (5th overtone crystal oscillator) as an LO, with the resulting IF sent to an SDR-IQ running *Spectravue* software.

To get measureable generated products within the 0 – 30MHz coverage of the SDR-IQ, only the following combinations were tested, with five of the nine possible multiplication factors tested :

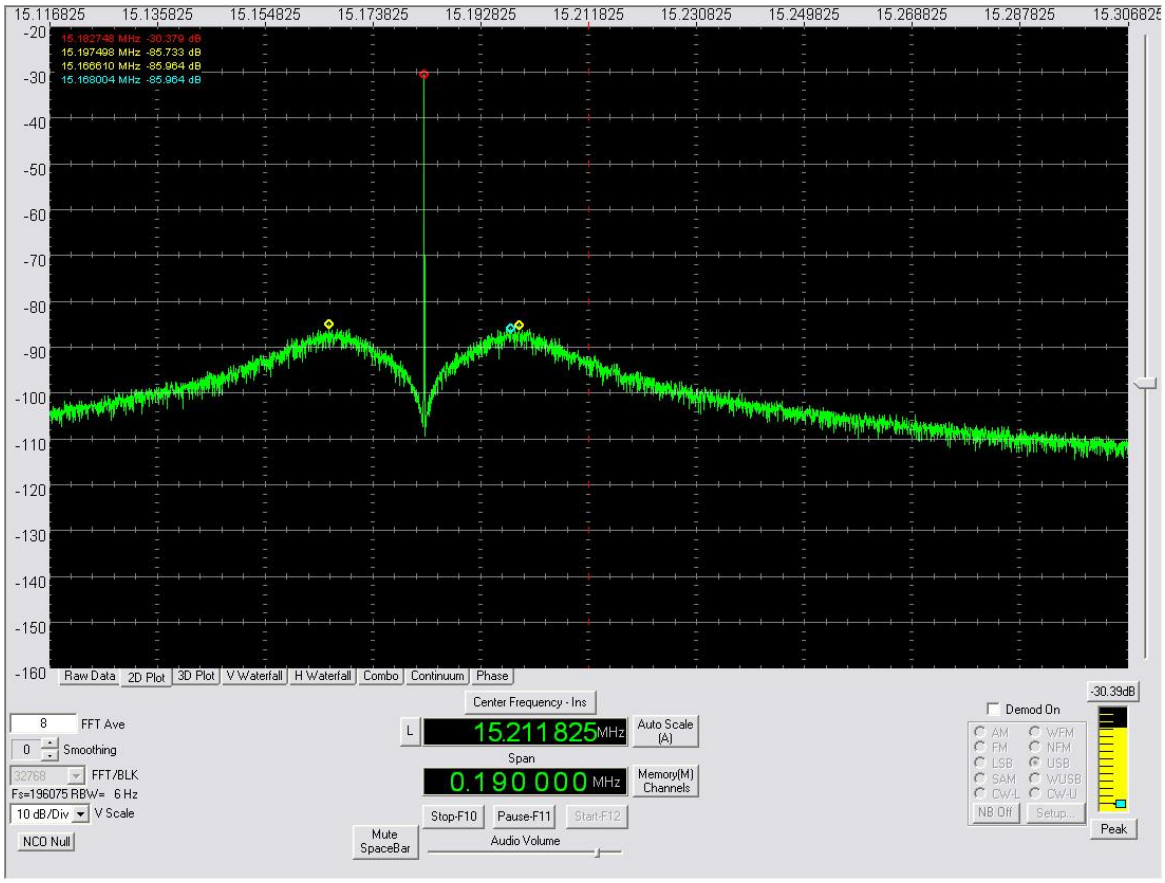
20.99MHz * 6	=	125.94MHz	- 116 = 9.94
20.99MHz * 6.25	=	131.19MHz	- 116 = 15.19
20.99MHz * 5.3125 [85/16]	=	111.509MHz	- 116 = 4.491
12MHz * 8	=	96MHz	- 116 = 20
12MHz * 2	=	24MHz	direct

All plots have a 6Hz FFT bin and Blackman Harris window, so noise bandwidth is about 14Hz with phase Noise in dBc/Hz about 11dB lower. Different input attenuation settings were used to compensate for the frequency respose of the converter – so absolute levels have to practical meaning. In all cases, phase noise at the edge of the plot was 10 – 20dB above the noise floor of the receiver / converter

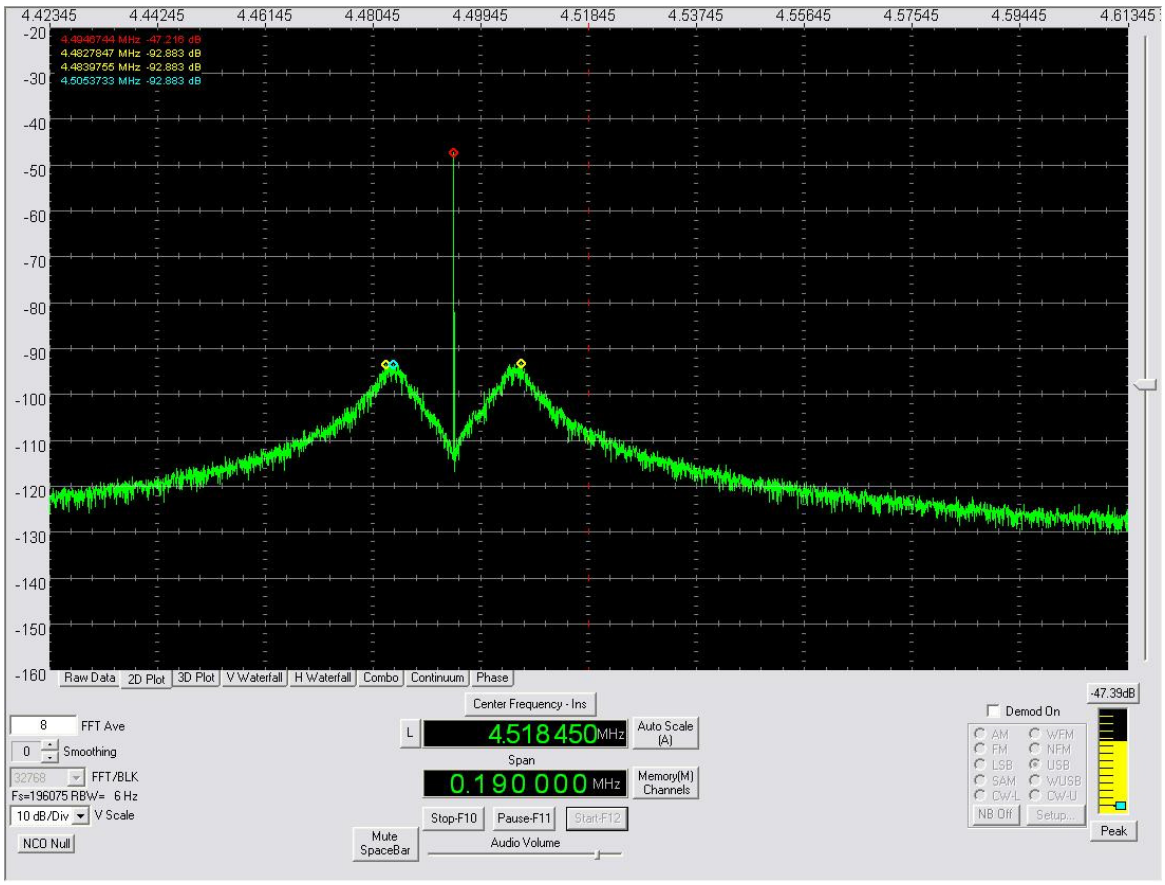
20.99 *6 = 125.94MHz



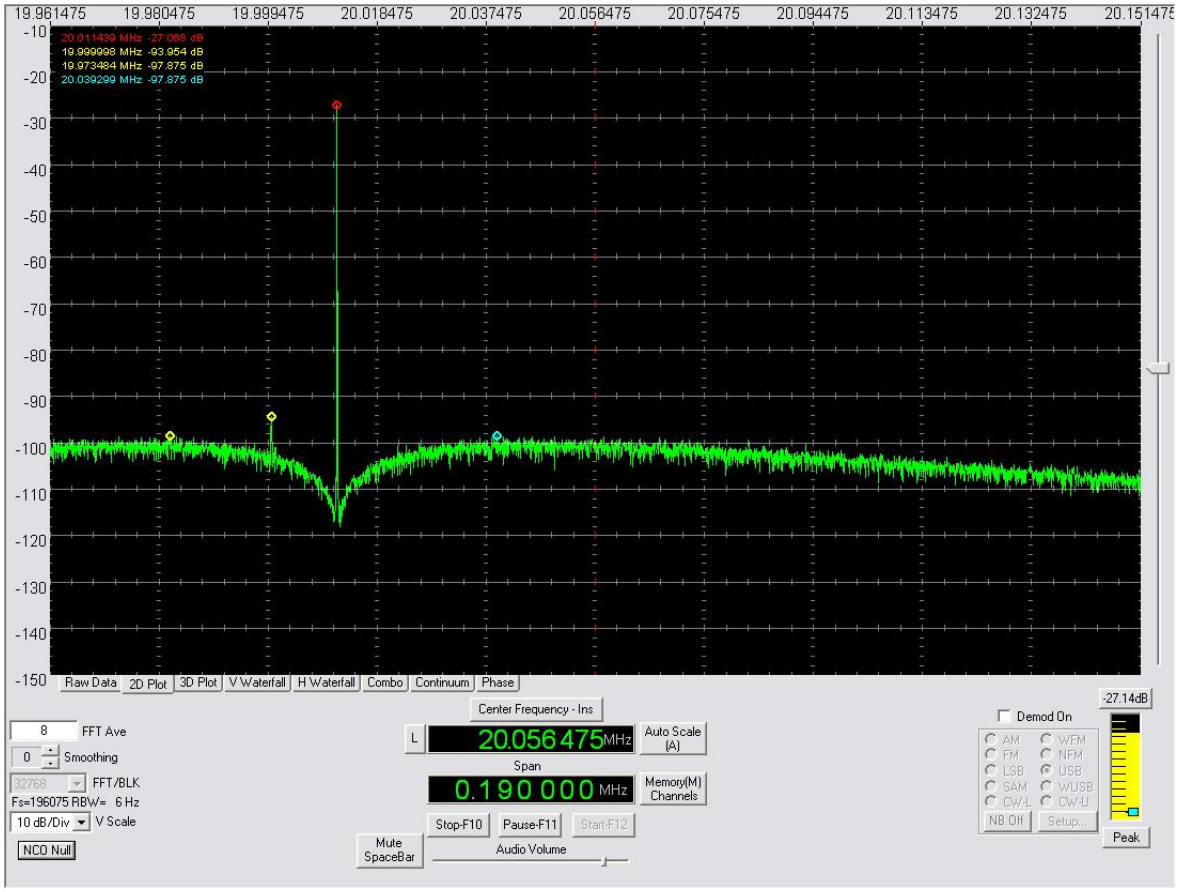
20.99 * 6.25 = 131.19MHz



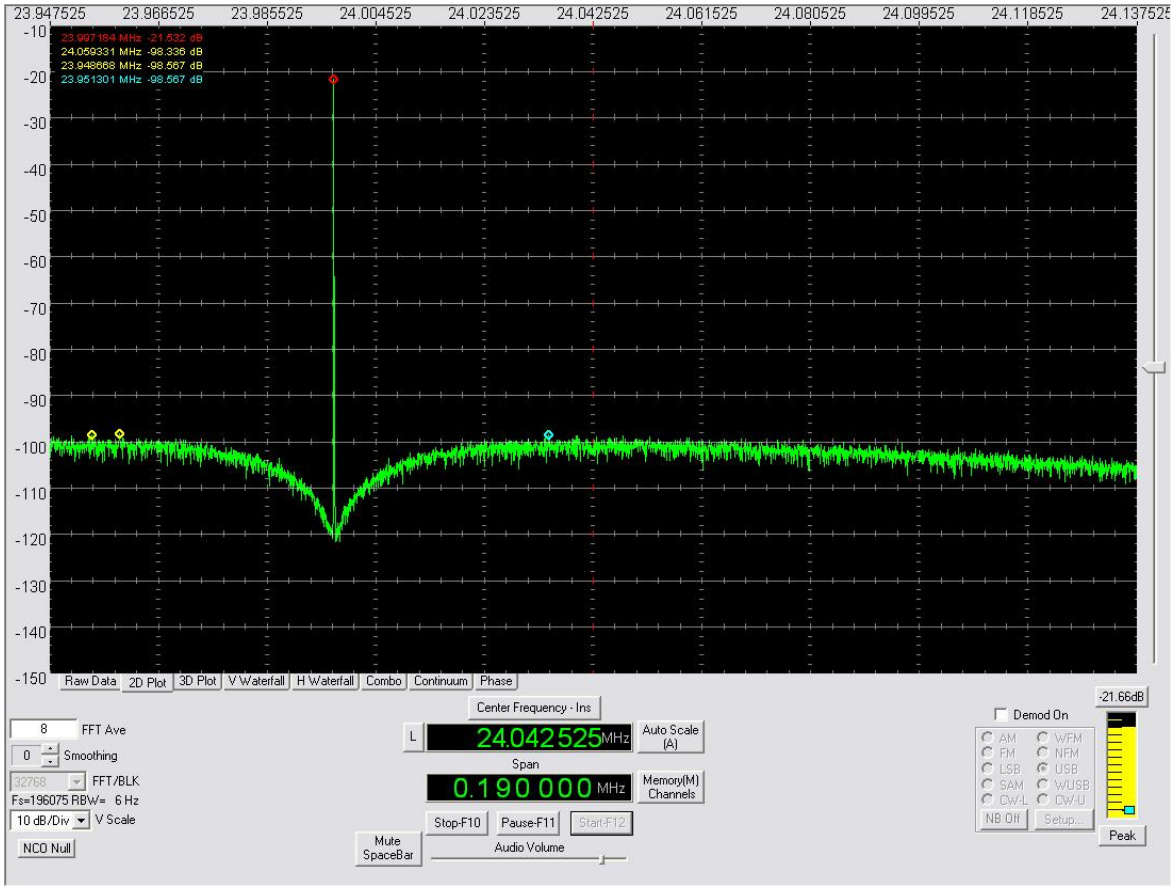
20.99 * 5.3125 = 111.509MHz

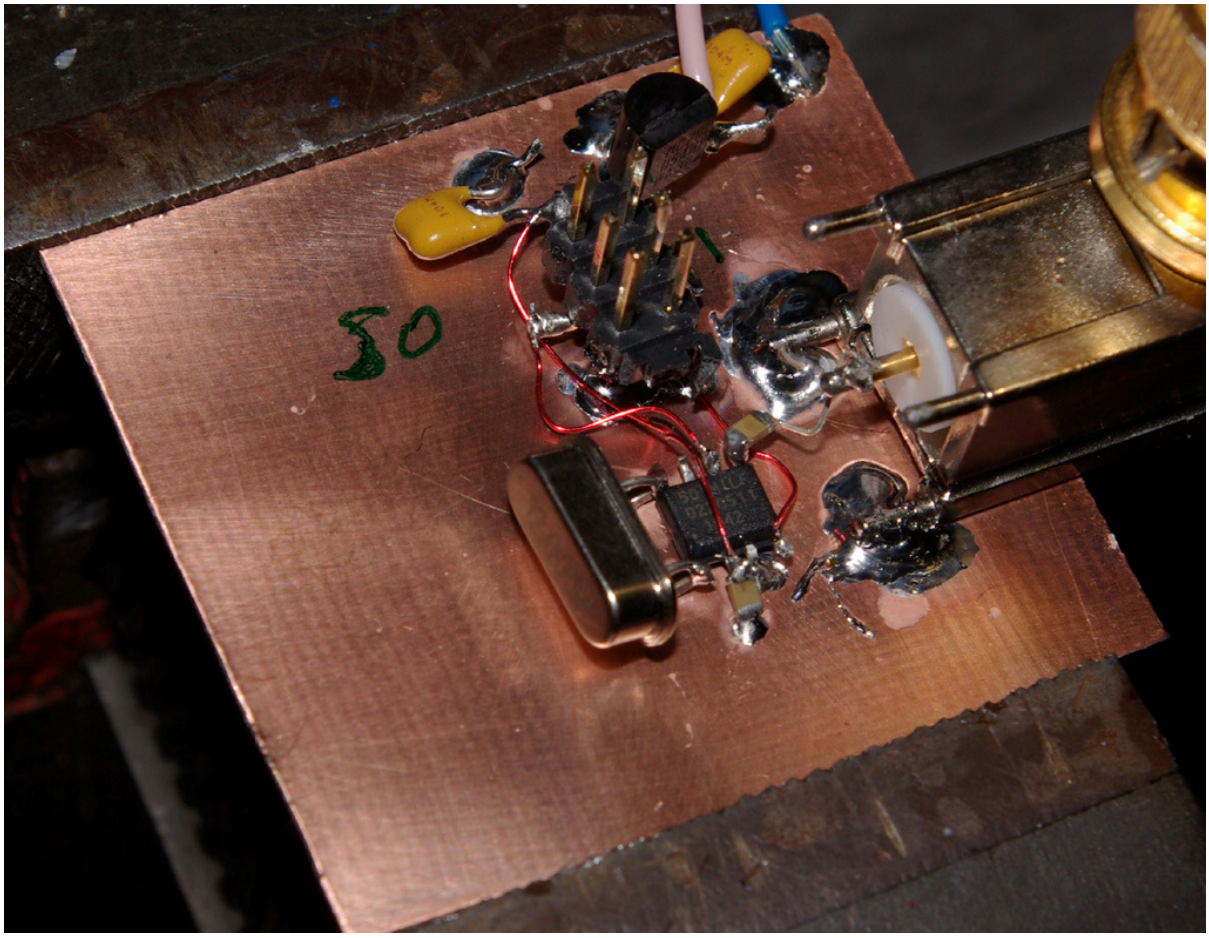


12 * 8 = 96MHz



12 * 2 = 24MHz





Test Breadboard