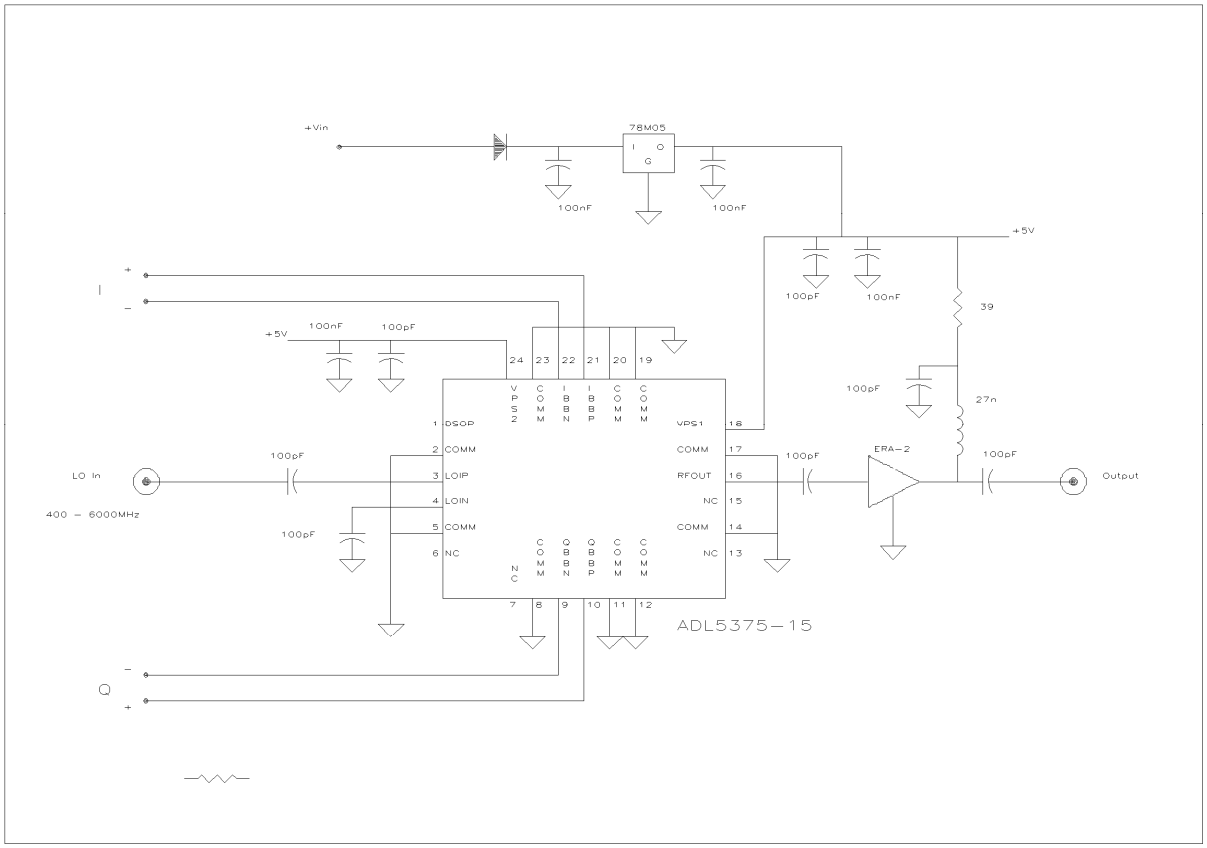
ADL5375 Quadrature Upconverter Tests

Andy Talbot G4JNT Feb 2017

Overview

The ADL5375 is a quadrature upconverter covering a frequency range of operation from 400MHz to 6GHz. As such it covers all the amateur bands from 430MHz to 5.76GHz. Two channels of quadrature I/Q baseband drive, which can have a bandwidth of up to 90MHz need to be supplied as a differential signal. RF at a nominal level of 0dB at the RF centre frequency is capacitively coupled to the input. The test module used for these tests includes an ERA-2 output amplifier. The circuit diagram is shown below

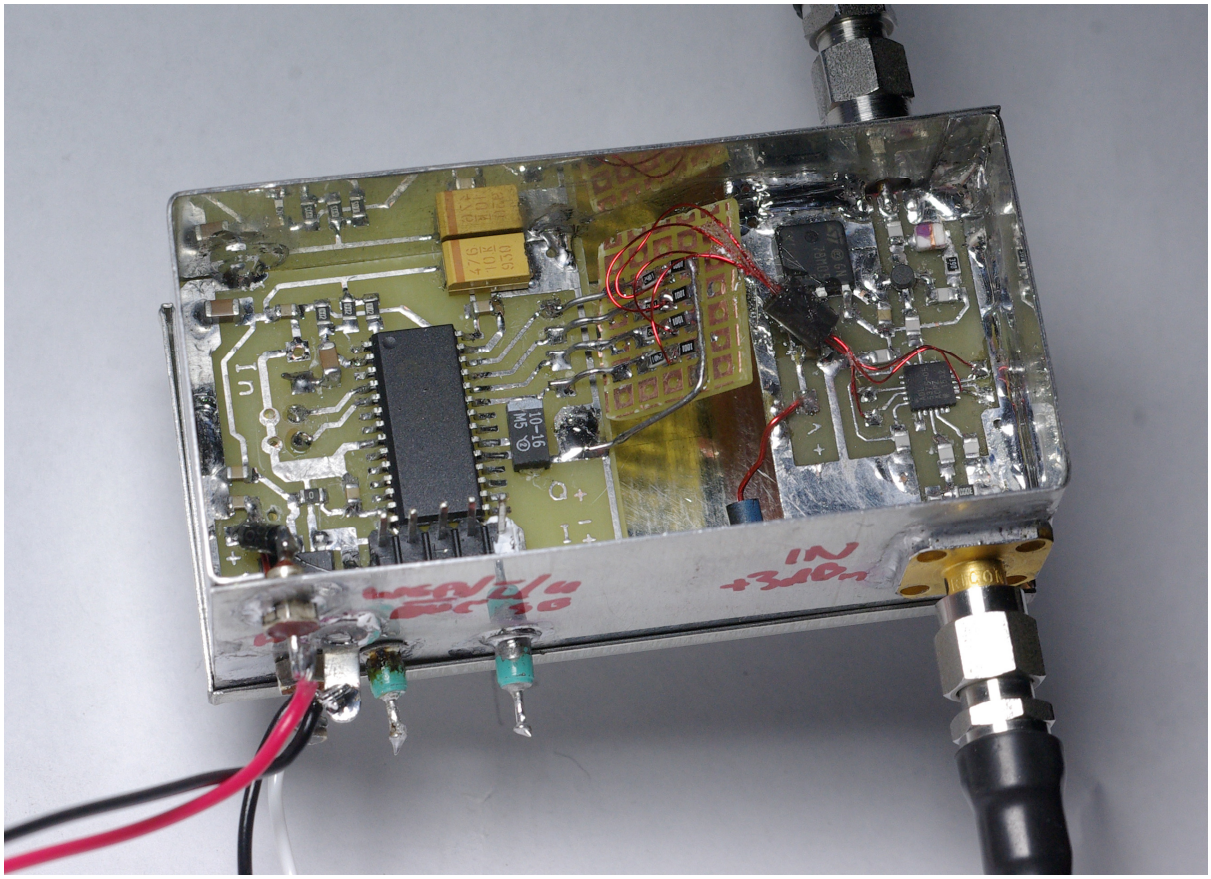


The differential I/Q drive is 1V peak-to-peak (or 0.5V pk-pk on each side) and can be generated by an opamp arrangement from single ended inputs, a differential line driver. or one of the many D/A converters and *dsPIC* devices with converters that supply differential outputs. Two variants of the chip are supplied, the ADL5375-05 and -15 version. The only difference is in the common mode voltage. The -05 version has to be externally biassed to a nominal 0.5V and the -15 variant to 1.5V. See later for the implications of using the wrong type!

Baseband Source

For these tests a *dsPIC* based frequency converter was used that has been developed by G8ASG. This takes in an audio waveform and down converts by 1700Hz, generating a folded-back audio spectrum from 0 to 1.5kHz for Weaver or third-method converters. Alternatively by pulling a pin low, it can be configured for I/Q drive with no frequency changing for a phasing type upconversion.

Output for I and Q channels appears as a differential voltage drive of around 1 V peak to peak on a common mode voltage of 1.76V. More details of the *dsPIC* converter can be found at [1] DC offset between the +/- lines of the I/Q drive signals can be adjusted in software to optimise carrier rejection, but does require the *dsPIC* MPLAB programming environment to be in use to allow this to be done in real time. Another pin, when pulled to ground, replaces the mixer drive with a DC level (its value can be defined in the *dsPIC* firmware) so that a plain carrier at the RF input frequency is generated.



Testing

Unfortunately the wrong device variant, the ADL5375-05 had been purchased and could not be optimally interfaced to the *dsPIC*. The common mode voltage delivered is incompatible with the -05 variant that needs around 500mV. It was therefore necessary to pot-down each of the four drive signals using 2.4k and 1k resistors (these are not shown in the diagram, but are visible on the bodge-board in the photograph). While the resistors drop the common mode voltage into the right region, they also attenuate the peak-peak drive voltage to around 0.3Vmaximum. This means there is a shortfall of 10dB in drive capability. As carrier rejection of the internal mixers is essentially independent of baseband drive level, the relative carrier rejection seen is therefore around 10dB worse than could be achieved with optimum drive levels. The tolerance permitted on the common mode voltage means a direct connection is permissible between the *dsPIC* and the ADL5375-15 variant of the chip.

A sinusoidal audio drive in the 300Hz – 3kHz region was supplied to the audio converter along with broadband noise for some of the plots. Noise drive allows the DSP filter response to be viewed. The following plots show the carrier and sideband rejection obtained for a range of operating frequencies.

NOTE : The sidebands seen at plus/minus 10kHz on some of the lower frequency plots are an artefact of the signal generator used and can safely be ignored.

Results

Up to around 1.3GHz, a carrier rejection of something like 40dB is achieved. At 2.3GHz this is beginning to degrade so that it shows about 30dB rejection ; at 3.4GHz a little over 20dB and at 5.76GHz, close to the upper specified frequency of the chip, only around 10dB can be seen. Although untested with this variant of the chip, carrier rejection at maximum output ought to be improved by perhaps up to 10dB if peak-to-peak drive is raised to 1V. No attempt was made to see if carrier rejection at higher frequencies could be improved by adjusting DC offset – perhaps at the expense of that lower down in frequency.

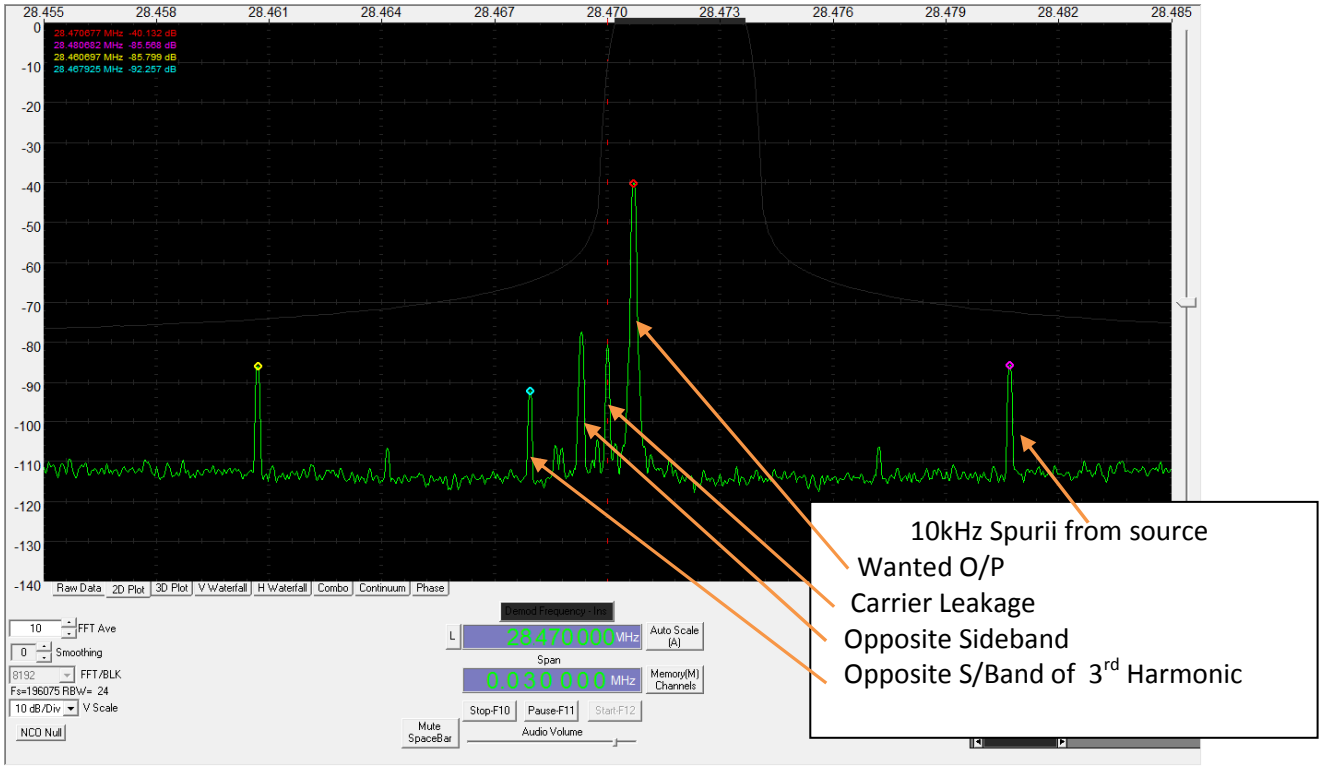
Opposite sideband rejection stays at a pretty-impressive 40dB up to at least 3.4GHz and only degrades to 30dB at the upper frequency limit, and to 38dB at 432MHz which is approaching the lower specified limit. Sideband cancellation is not a function of drive, so won't change with the correct chip variant. Since the I/Q drive signals were generated by DSP and, apart from DC offset which was set at test, are near enough identical. So no attempt was made at amplitude tweaking I and Q channels to get a better sideband rejection .

The Third harmonic Image Conundrum

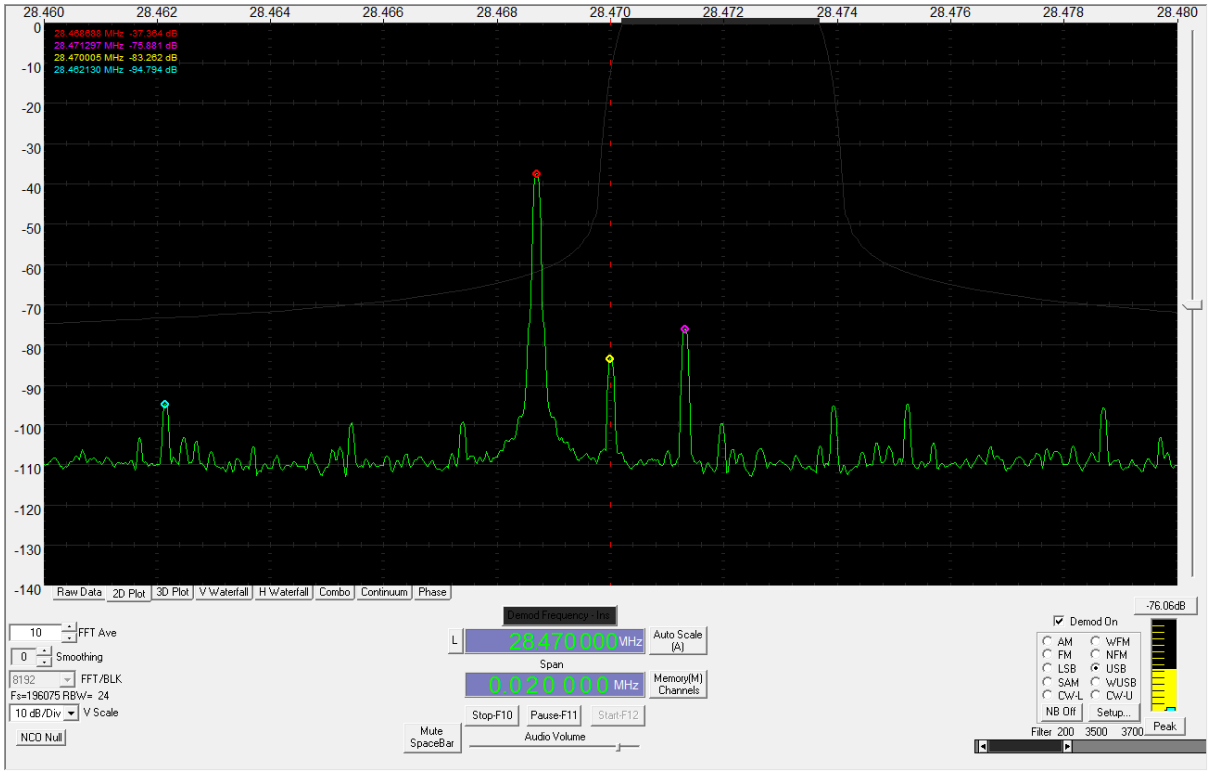
All practical phasing (and Weaver) converters can exhibit a somewhat surprising and annoying spurious artefact. If there is any alternate odd order harmonic distortion, 3^{rd}, 7^{th}, 11^{th} etc. present in the I/Q drive to the mixers this will appear uncancelled on the opposite sideband. Consider a 400Hz tone at 0° and 90° fed to the mixer. Its third harmonic will lie at 1200Hz. The phase between the two harmonic signals is multiplied by the harmonic and will therefore be now 270° This is the same as -90° and leads to this harmonic component giving an uncancelled sideband on the opposite side to that of the wanted conversion. So if the wanted signal is 400Hz above the carrier, the third harmonic lies 1200Hz below it. Fifth harmonics will wrap round to 90° and be cancelled, but 7^{th} and 11^{th} harmonics will appear

This artefact can be seen on some of the plots below. The first plot, at 432MHz (with the products labelled) was deliberately overdriven very slightly to emphasise this component. All the others, driven properly, show it at least 50dB and typically 60dB down, illustrating the high quality of the sinusoidal signal delivered by the *dsPIC* source.

Spectrum Plots

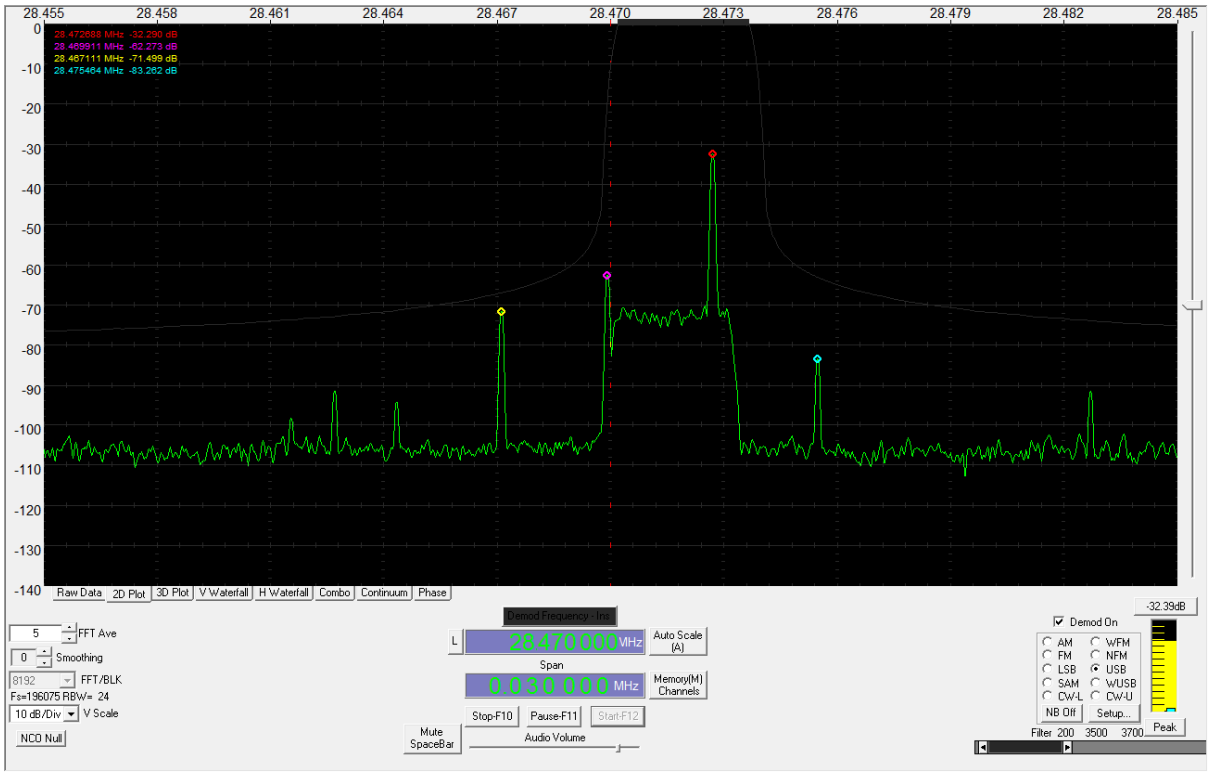


F_{RF} = 432MHz , Drive 2.4kHz tone, Weaver (third method) conversion (very slight overdrive)

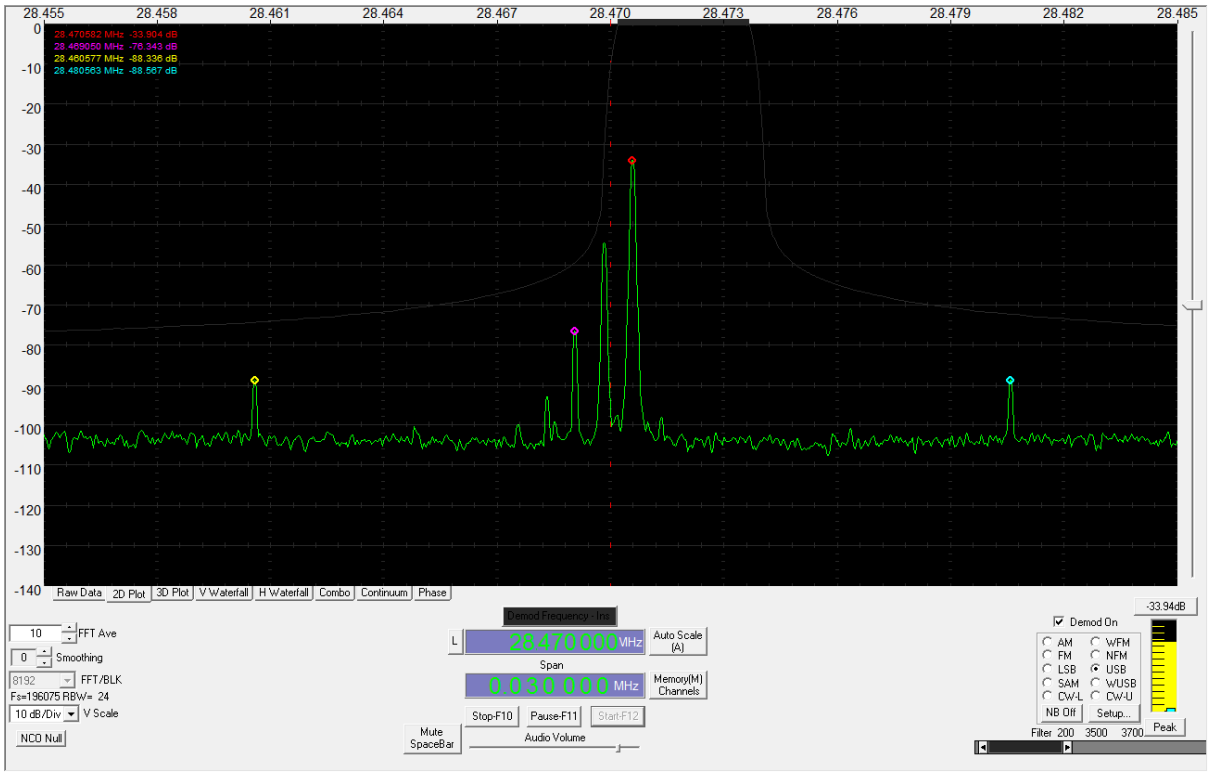


F_{RF} = 1296MHz Drive - 400Hz Tone Weaver Mode

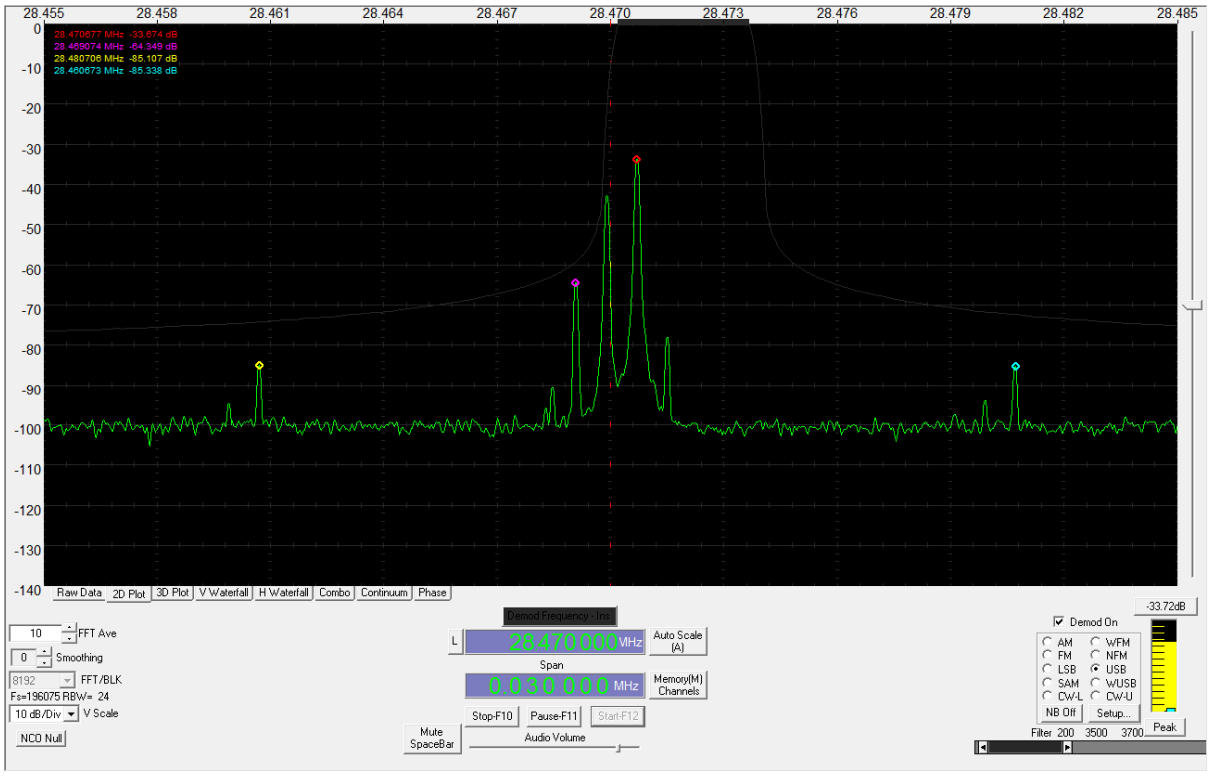
F_{RF} = 1296MHz With drive consisting of 2.1kHz tone plus broadband noise, Weaver conversion



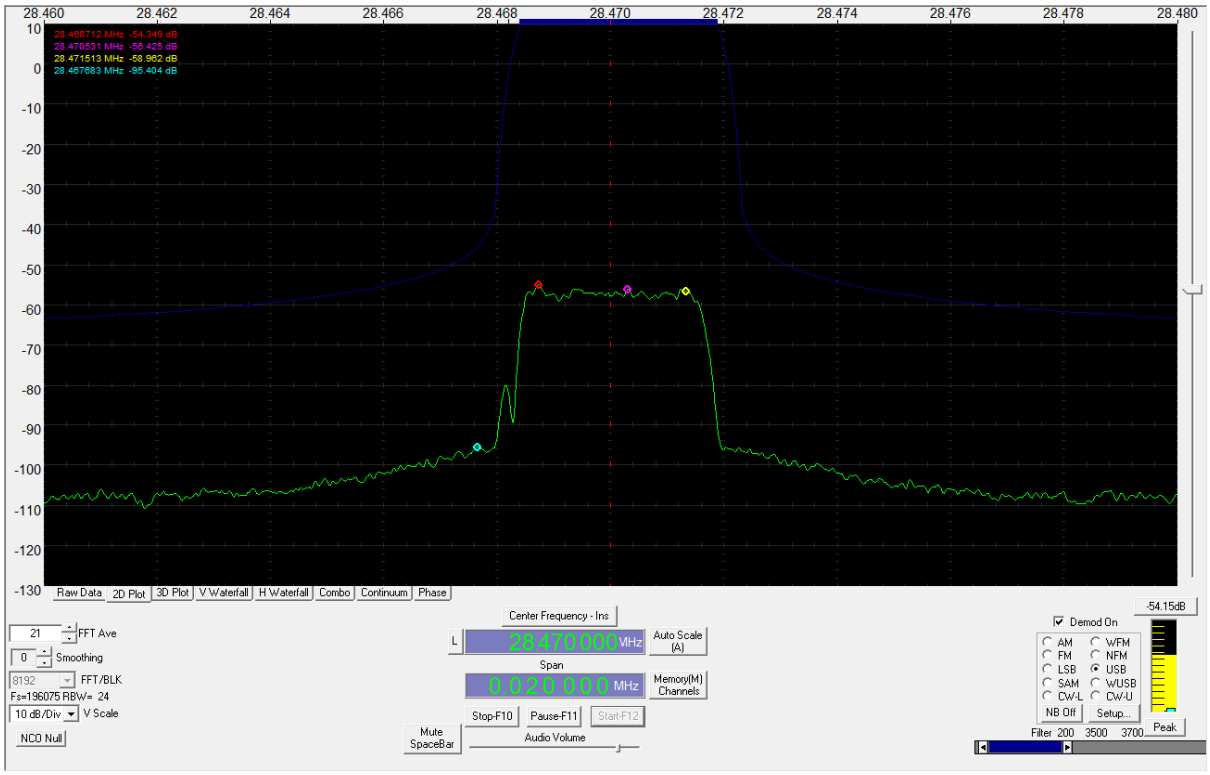
F_{RF} = 2320MHz Drive = 2.7kHz Tone and broadband noise, Direct upconverter mode.



F_{RF} = 3400MHz Drive = 2.3kHz Tone Weaver converter mode



F_{RF} = 5760MHz Drive = 2.4kHz Tone Weaver Converter



F_{RF} = 1296MHz Drive = broadband noise, Weaver conversion

Conclusions

The opposite sideband rejection of 40dB is more than adequate for casual use on the higher microwave bands when used as a conventional Upconverter where it lies 3kHz to one side. At HF this level of adjacent channel is verging on unacceptable if used at high powers. When used as a Weaver source, this unwanted sideband lies on top of the wanted signal and will be completely 'invisible'.

Carrier leakage values shown ought to be improvable with proper DC level matching in the chip drive. At the lower frequencies, the 40dB value seen is good, and even at 20dB at the upper frequency ranges should not cause any problems. In Weaver mode this appears as a 1700Hz tone in the passband, noticeable but not usually objectionable on SSB voice, and insignificant when used with data modes.

The 'ideal' I/Q source now possible using the G8ASG *dsPIC* code means the full capability of modern quadrature Upconverters can now be tested. Being able to generate a respectable USB signal using this arrangement, in conjunction with a single chip Fract-N synthesizer like the ubiquitous ADF4351 or LMX2541 should lead to some interesting UHF or microwave transmitter and beacon ideas.

There are now several single chip solutions containing both Fract-N synth and quad Upconverter; look at the Analog devices ADRF67xx family, for example. A PCB containing one of these and *dsPIC* could make a useful standalone module for developers…

References

[1] G8ASG *dsPIC* Audio Converter http://www.g4jnt.com/*DsPIC*_Weaver_DUC.zip