Initial Musings and Tests on Breadboard Locked Beacon Sources for 432MHz

Andy Talbot G4JNT May 2010

Introduction

The reverse DDS concept for locking microwave sources has proved itself by now, having been used successfully on the Bell Hill 3.4, 5.6 and 10GHz beacons. Being DDS based, arbitrary frequencies can be generated to high accuracy, and constant amplitude data modes like JT4 and JT65 can be incorporated. An off the shelf module is available as a kit from G8ACE / G4NNS for retrofitting to such beacons. [1] JT4 modulation can be added by changing the PIC controller and adding a suitable timing source (a GPS module)

At 432MHz the RDDS concept is not so easy to use. While the RDDS module allows construction of a straightforward locked source, the lower times-four frequency multiplication means that Frequency Shift Keying for either CW or JTx now has to pull the PLL over a wider range in excess of 300Hz for JT65B - the preferred mode for VHF/ UHF beacons - leading to sluggishness and chirpy keying. Also, the 32 bit DDS used in that module leads to a frequency setting resolution of 0.6Hz which is on the edge of being a bit marginal for JT65B operation with its 5.5Hz tone spacing.

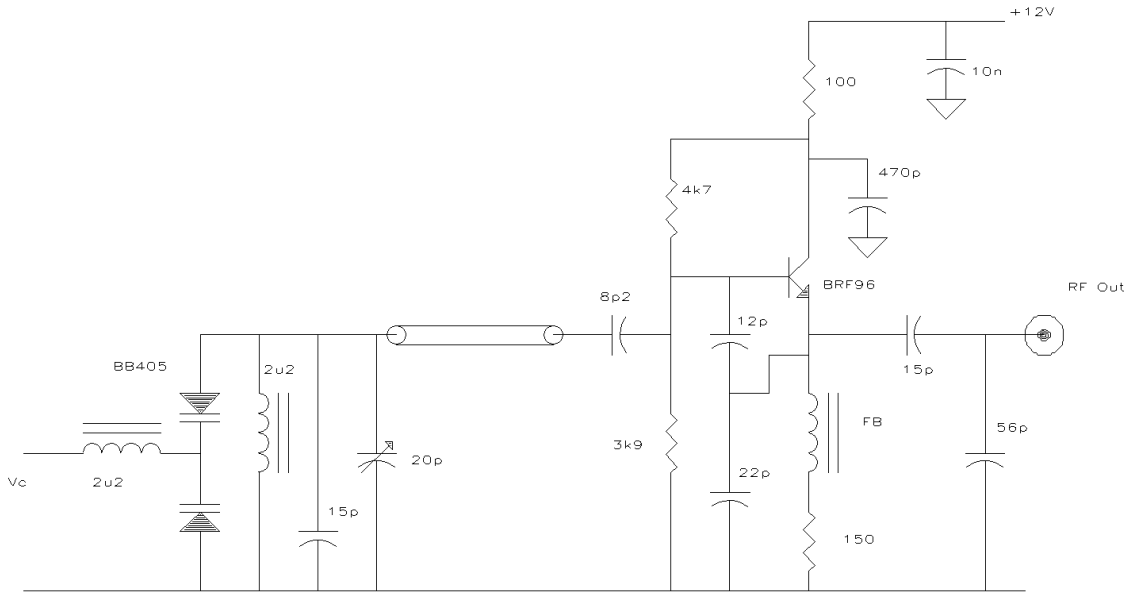
The following are my results of initial tests to find a more suitable source for 432MHz beacons

For all these experiments, a fixed semi-arbitrary frequency of 432.43MHz was adopted as a common reference for comparison.

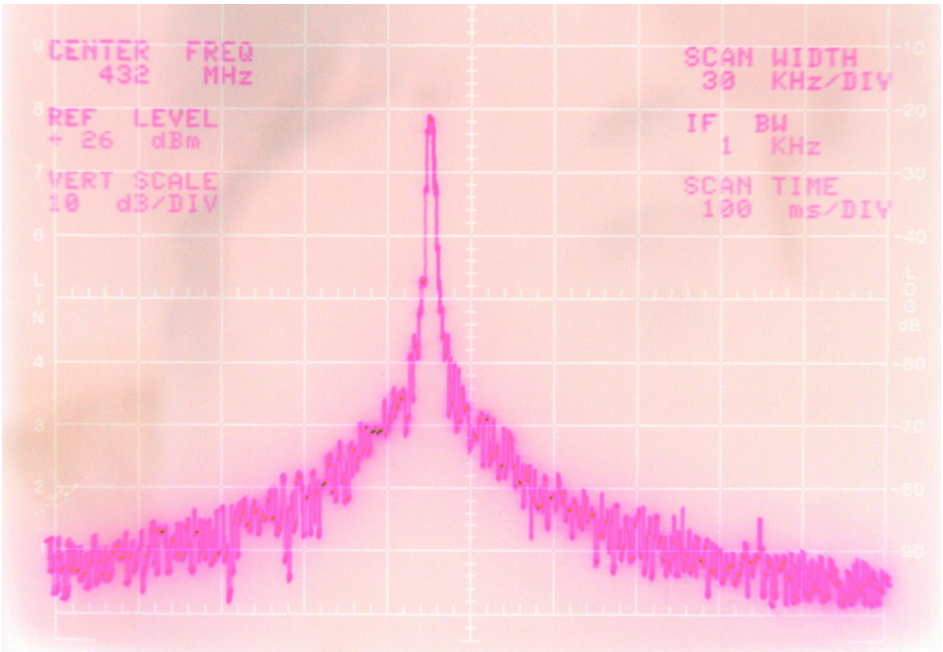
RDDS Using LC Oscillator

To increase the modulation bandwidth, a coaxial-resonator VCO was constructed at 216MHz to clock an AD9852 DDS programmed to supply an output at 10MHz when the VCO was running at 216.215MHz. The DDS output was then compared in phase with a master 10MHz reference using an NE612 mixer and op-amp PLL filter, the output being fed back to lock the VCO. The final RF would be supplied by frequency-doubling the VCO output.

The Coaxial resonator VCO whose circuit is shown below (component values are for the later 432MHz version) was chosen to exhibit a low level of microphony and have a low voltage tuning range coupled with a high inherent stability to avoid having to have too wide a lock / tracking range for the PLL



A spectrum plot of the oscillator in free-run mode can be seen showing that far-out phase noise – where it will be unaffected by the PLL – can be seen to be around at least -100dBc at 100kHz from the carrier. In fact the phase noise of the spectrum analyser itself is influencing the reading and the actual figure is rather better than this – probably more like the -110 to -115dBc/Hz shown in the later plots of the locked source.. The PLL was designed for 100kHz bandwidth, this being considered a reasonable value to ensure the VCO would not drift out of lock.



Results of the LC tuned RDDS were very unsatisfactory. The wide bandwidth allowed close in spurious products from the DDS to get through with consequent increase in relative amplitude by the square of the frequency multiplication, leading to spurious products at levels as high as -30dBc. Passing the DDS output through a 10MHz crystal filter to clean it up failed as this narrow filter is now inside the PLL loop reducing its bandwidth to a few tens to hundreds of Hz and killing any ability to maintain lock.

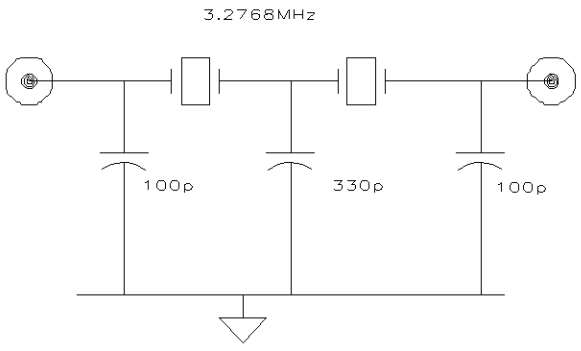
Conclusion - abandon RDDS concept with LC oscillator

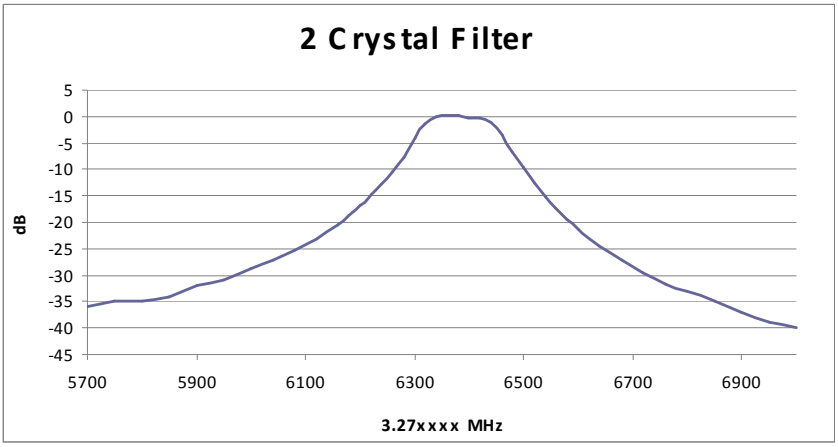
PLL Multiplier

On the GB3SCS 2.3GHz beacon a different approach had been taken, just out of interest and to try the technique of PLL multiplication. Details can be found at [2], and involved using a DDS source to generate a reference that is subsequently multiplied using a conventional synthesizer based around an LMX2346 and packaged VCO, a combination that fortunately happened to be to hand

The synth chip offers the possibility of arbitrary multiplication by any non-integer value that is a ratio of two arbitrary integers, within reason, by programming the N and R dividers appropriately for a comparison frequency that only needs to be close to a target design value. This means the DDS output can be at virtually any frequency, and choosing one that can be filtered by low cost off the shelf crystals is an obvious choice. Clearly, filtering is essential as, again, the PLL bandwidth will have to be reasonablywide. On GB3SCS a suitable frequency using a 2.4576MHz baud rate crystal was found. [3]

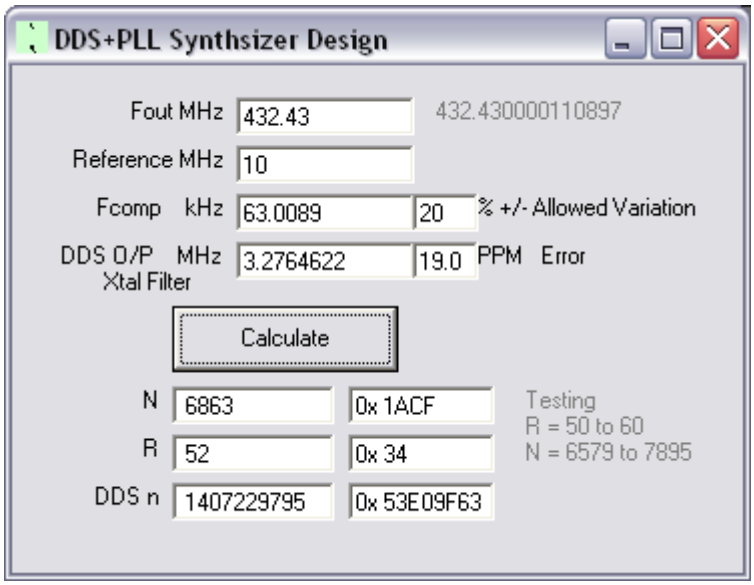
A bag of about a hundred 3.2768MHz crystals had serendipitously been purchased at the recent Andover Boot Sale, so this was the obvious choice for the DDS output. A two-crystal filter was put together and its response can be seen below. The centre frequency is 3.2764MHz and there is scope for about 40ppm variation on this in either direction.





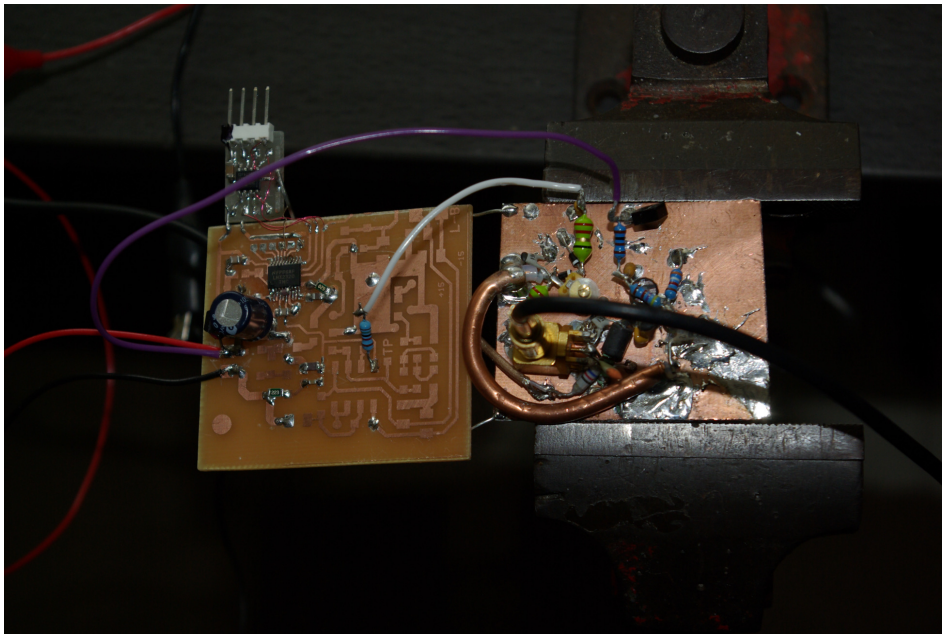
With a wide choice in N and R values for the PLL, and an 80ppm range of variation, several frequency solutions become viable. A design utility was written to allow DDS frequency and tolerance to be specified and an approximate Fcomp. It would then go away an search for the most suitable R and N values.

For 432.43MHz, with an Fcomp around 60kHz the resulting values were generated.

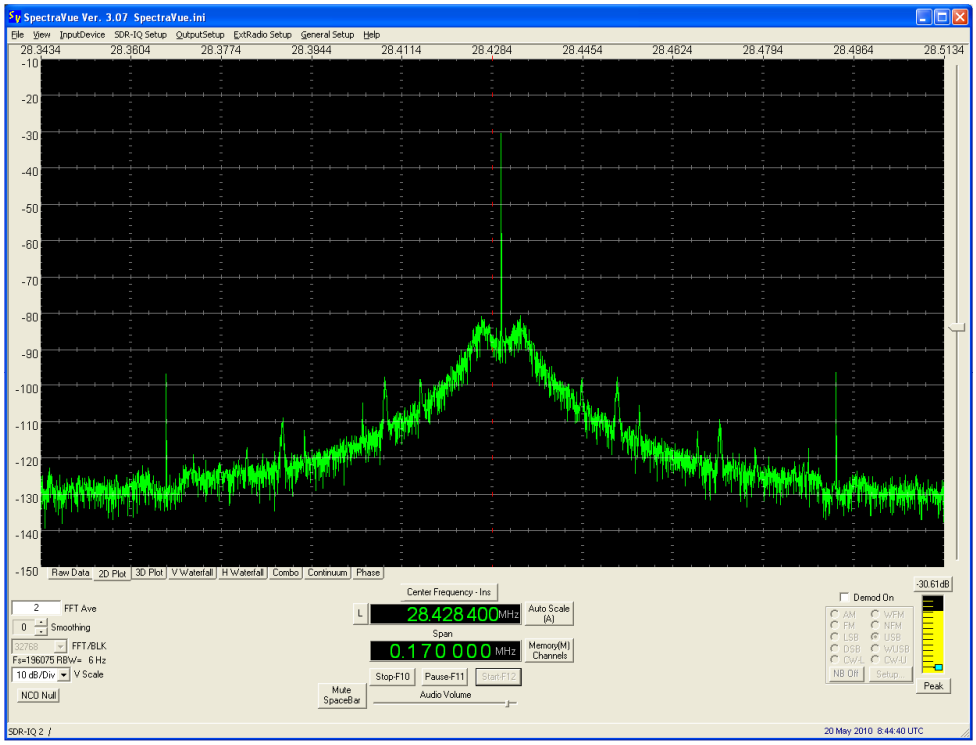


Initially an already existing 350 – 480MHz synth module using a packaged Minicircuits VCO and LMX1501 chip was tried. Although a clean output could be obtained, phase noise and spurious sidebands were unacceptably high due to the wide tuning range of the VCO and the performance of the now rather-long-in-the-tooth chip.

The coaxial resonator VCO was rebuilt for 432MHz operation and used to clock an LMX2320 synthesizer chip, several of these devices being to hand. All construction was using breadboarding techniques, using a PLL PCB from an earlier project and birds nest construction as shown in the photo. After some fine tuning of PLL parameters such as reducing the PLL bandwidth to 5kHz and adding additional filtering on the DDS output signal, results eventually proved quite acceptable. All plots were made using a 432 MHz converter feeding an SDR-IQ to look at signals in a bandwidth out to 170kHz away.

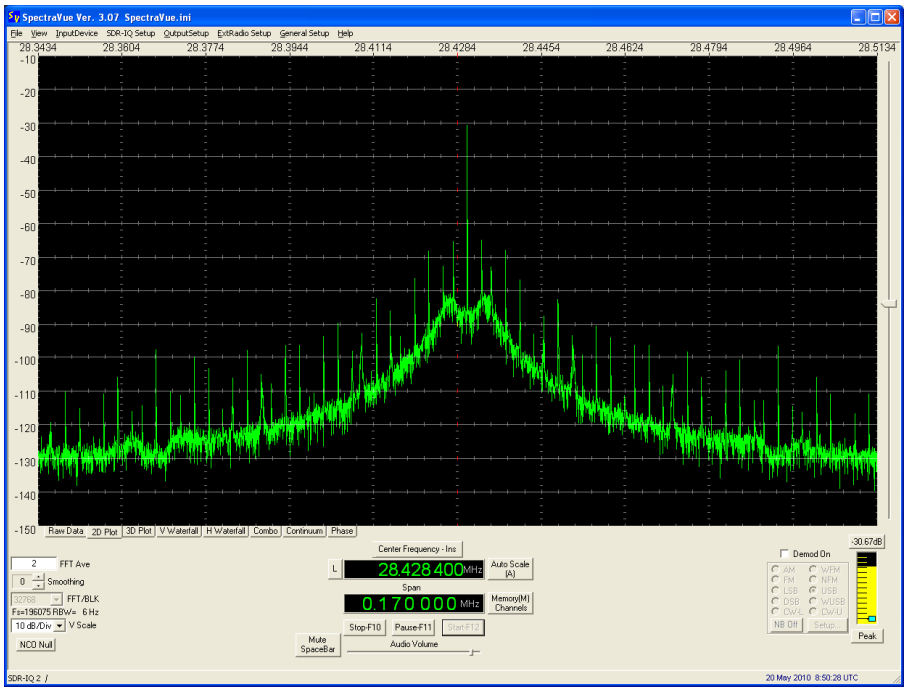


First plot used a Rhode and Schwarz synthesizer instead of the DDS to provide a comparison reference for subsequent texts with DDS sources. FFT bandwidth is 6Hz. Note the comparison frequency sidebands at +/-60kHz at a level of -65dBc. Although just off the screen, phase noise at 100kHz spacing is in excess of 110dBc/Hz and barely within the measurement capability of this system – it may be better.

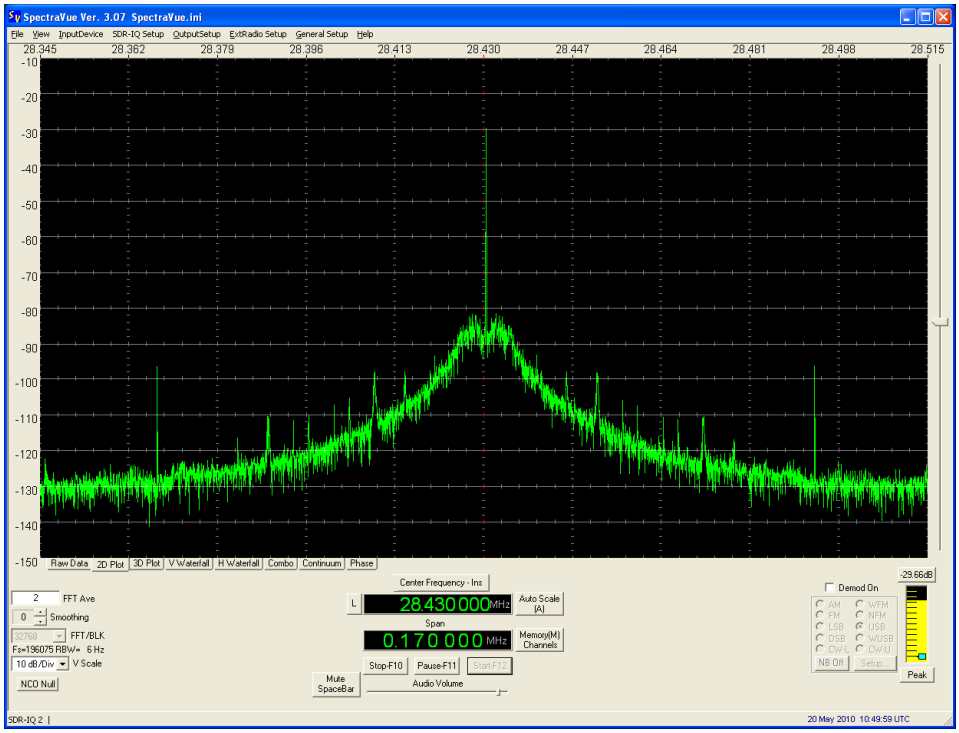


This plot is using the DDS clocked at 10MHz using just the two-crystal filter (no additional LPF)

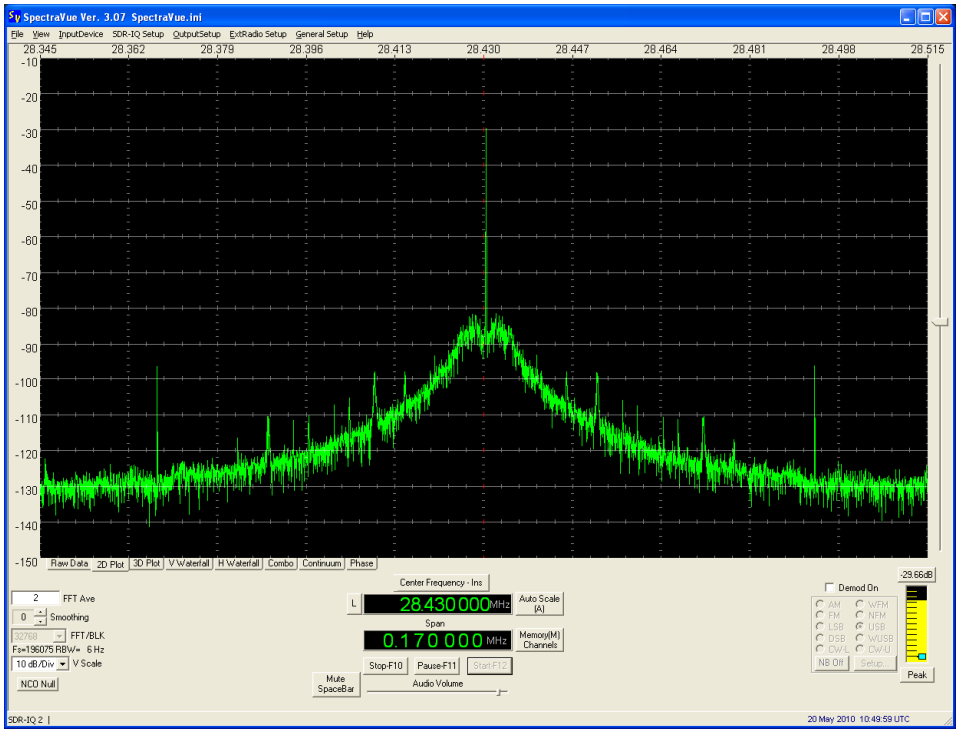
To remove spurious components. Note how dirty the result is with the DDS clocked at 10MHz to generate 3.27MHz. As the generated frequency is getting close to the Nyquist limit, spurii increase and even with the limited filtering performance of the crystal filter is insufficient to remove these.



By using the DDS's own clock multiplier to go to 40 or 50MHz, a much cleaner output results in spite of the tiny increase in phase noise due to the low-spec PLL multiplier inside the chip. (Exactly reflecting the findings on GB3SCS). Here the DDS clock multiplier is used to clock the device at 50MHz. Note the significantly reduced spurious levels at -70dBc (ignoring the reference frequency sidebands)



The PLL bandwidth was then reduced to 5kHz in an attempt to further clean up the spurii. As can be seen, there was very little change.



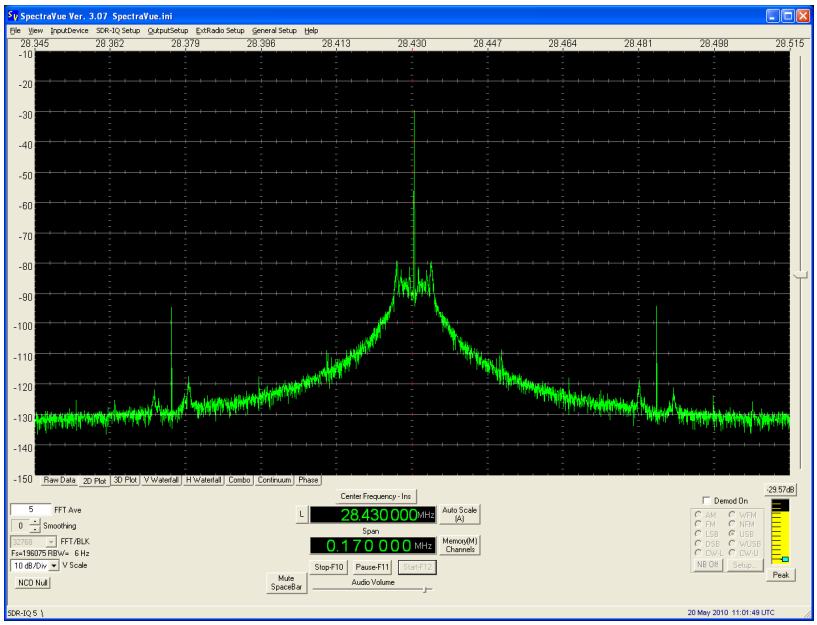
For a final check, another set of R and N values with a slightly lower Fcomp value was selected with appropriate change to the DDS output frequency.

Requested Fout = 432.43MHz

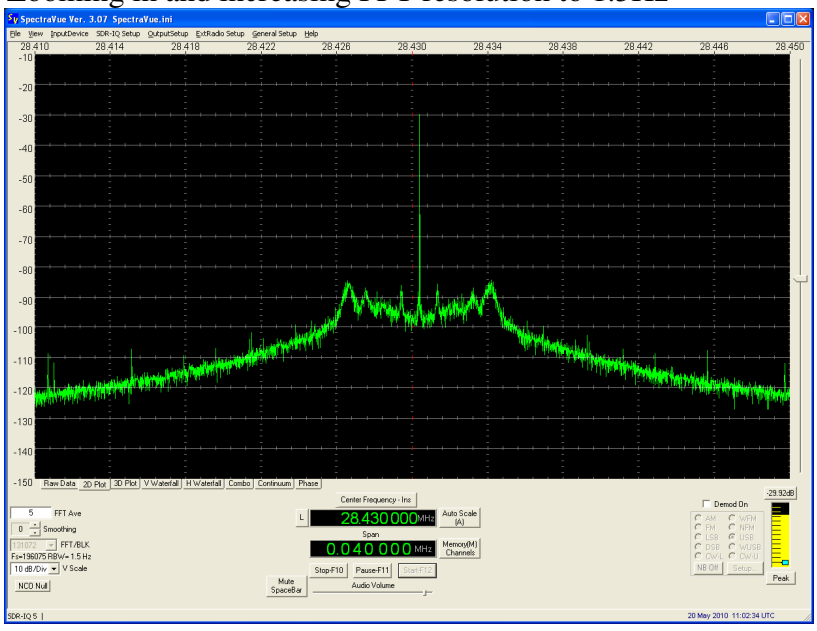
DDS 10MHz Fref in * 5 Internal clock multiplication
FDDS = 3.2763985MHz N DDS = 281440491 0x 10C670EB (to 32 bit approximation, 0.8Hz resolution)

N PLL = 7919 R PLL = 60 Fcomp = 54.6066 kHz

No correction was made to the PLL filter components, and as the plot shows, there is a consequent worsening of close in phase noise showing as a peak at the loop bandwidth either side of the carrier – a result directly attributable to the non-optimised filter. However, even so, a noticeably cleaner spectrum is observable – apart from the reference sidebands staying stubbornly at around -65dBc !



Zooming in and increasing FFT resolution to 1.5Hz



Conclusions

The breadboard results suggest a DDS and PLL multiplier will allow a source form432MHz beacons that will meet the requirements for close-in spurious and phase noise suitable for a demanding urban environment.

The next stage will be to build a source to a higher standard of construction, in a screened enclosure with all critical signals suitably bypassed instead of the open breadboard here. This will hopefully reduce spurious components to an even greater degree.

There is still scope for improvement of spurious levels, but will need the better screening and layout of a proper engineering model to allow meaningful results to be obtained.

References

[1] Reverse DDS Module http://myweb.tiscali.co.uk/g4nns/RevDDS.html

[2] GB3SCS frequency Locking http://www.scrbg.org/TheNewGB3SCS.htm

[3] Interestingly, a filter tested using 2MHz crystals with a passband / reference at 1.99997MHz turned out to be unsuitable for an unexpected reason. Being so close to a subharmonic of the DDS reference input at 10MHz lead to DDS spurii separated by only 30Hz from the carrier. These were too close to the wanted signal to be filtered by the crystal. No such problems were found using 2.4576MHz.