Locked Beacon Sources for 432MHz

Andy Talbot G4JNT June 2010

Introduction

Reference [1] describes initial designs for a locked beacon source for 432MHz, and shows preliminary performance of a lashed-up breadboard DDS followed by a PLL multiplier that showed a potentially promising performance. That was put onto a properly designed PCB with considerable attention paid to decoupling of supply lines and the critical VCO control voltage from the synth chip. The two-crystal filter for the 3.2764MHz input reference was incorporated on this PCB

Coaxial Resonator VCO

The first version used the same coaxial resonator VCO and PLL values as the original breadboard. But results were not very satisfactory. At the suggestion of G4DGU, the resonator element was changed for one chamber of a UHF helical resonator – readily available off the shelf and use din most UHF radios. A number of surplus recovered units were to hand – in normal bandpass filter use they will tune over at least 425 – 4760MHz. As the bottom (ground) end of the resonator is bought out to a separate pin, making the unit a two port device, the same bottom end tuning using a high variable capacitance diode could be used, and the PCB would need little surgery to accommodate the resonator in place of the coaxial loop. The breadboard version worked immediately, and juggling with capacitor values allowed the unit to be brought onto frequency where it proved to be remarkably stable and 'clean sounding'
The phase noise plot of it in free run mode, with a very well decoupled Vc line can be seen in Figure 1. This plot has a 12Hz noise bandwidth, and the resulting phase noise at 20kHz offset works out to be around -110dBc/Hz.

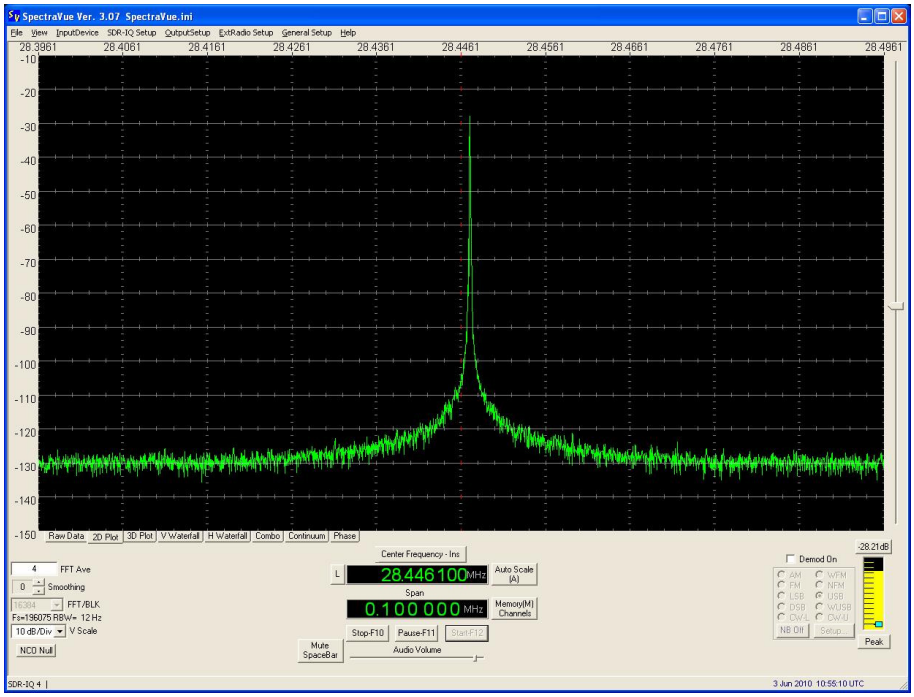


Figure 1 Helical Resonator VCO - Free Running

Using the PLL parameters derived earlier, Fcomp = 63kHz and a loop bandwidth of 6kHz gave the rather unsatisfactory phase noise plot Figure 2 . The loop bandwidth is too low, and residual noise is degrading the VCO. The VCO tuning with the bottom end tuning was very non linear, with the sensitivity varying from 2MHz/v at Vc = 1V to 500kHz /V at 5 volts tuning. This 4: 1 range prevented an optimum solution from being found for the PLL filter, and the phase noise plot changed appreciably as the VCO centre frequency was adjusted. Not satisfactory

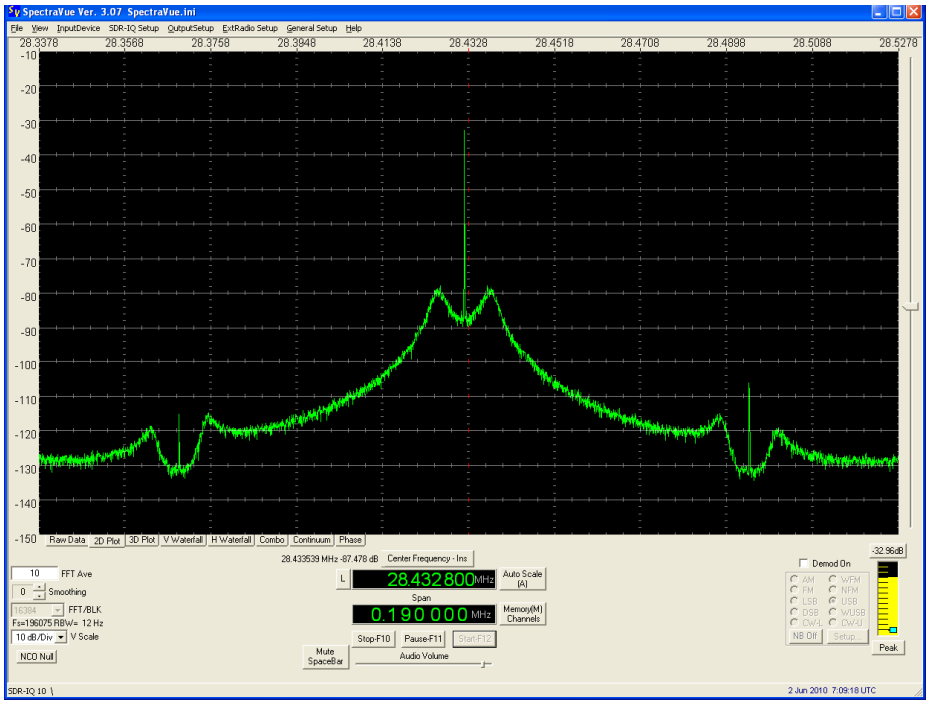


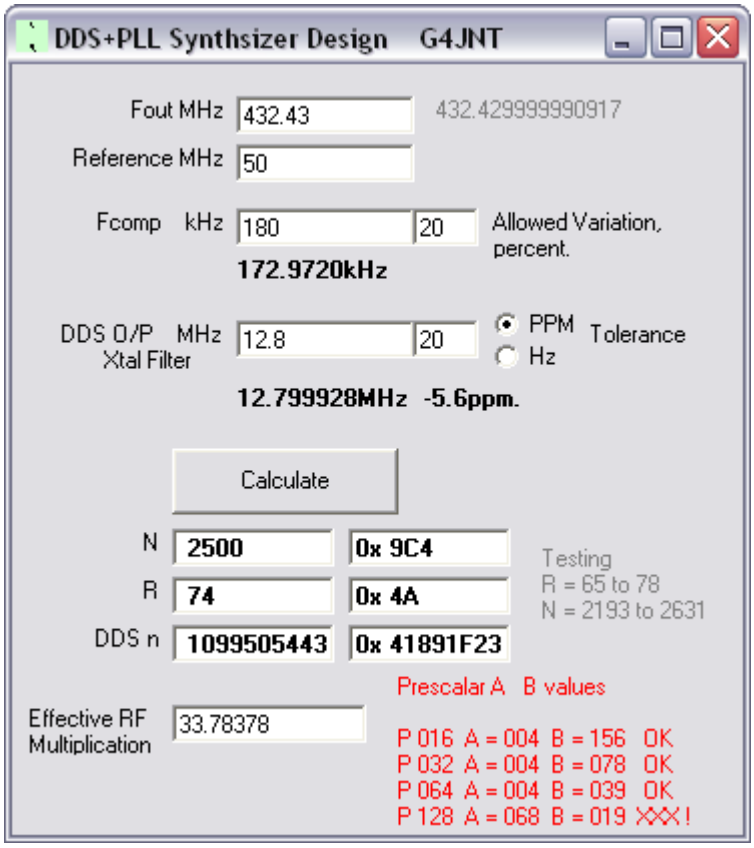
Figure 2 Phase noise plot of initial PLL design

The solution was to aim for a higher Fcomp which would in turn allow a higher lop bandwidth. No solution could be found using the 3.2764MHz Reference input so this was changed to 12.8MHz where there is more scope for fining suitable R and N divider ratios. Another crystal filter was made up – this time using a single crystal in parallel resonance combined with the DDS filtering. It was decided to keep this separate from the PLL PCB to allow for future changes without hacking the PCB too much – so the existing one was removed and bypassed.

A solution was found for Fcomp = 172.972kHz R = 74 N = 2500 (A = 4, B = 39). The design software suggests other values with slightly higher Fcomp values ought to be possible, but attempts to programme these into the PLL failed – the PLL would not lock to the correct frequency.

The problem turned out to be the apportioning of the N divider ratio between the A (prescalar swallow counter) and B dividers for the variable modulus divider in the LMX2320 chip. The total division ratio N is formed from N = A + P.B where P is the prescalar which can take on values of 128 or 64 for this device.

But B must be greater or equal to A and several initial solutions did not allow this. The PLL divider design utility was subsequently modified to test for a valid N value.



PLL filter values were calculated for a loop bandwidth of 16kHz which was about the widest that was possible with this VCO. To achieve a higher bandwidth required a higher tuning sensitivity on the VCO, and this was redesigned to the circuit shown in Figure 3 where the bottom end varicap tuning was abandoned and a more conventional lightly coupled UHF varicap pair used instead. These have a higher Q and resulted in a marginal phase noise improvement in free run mode.

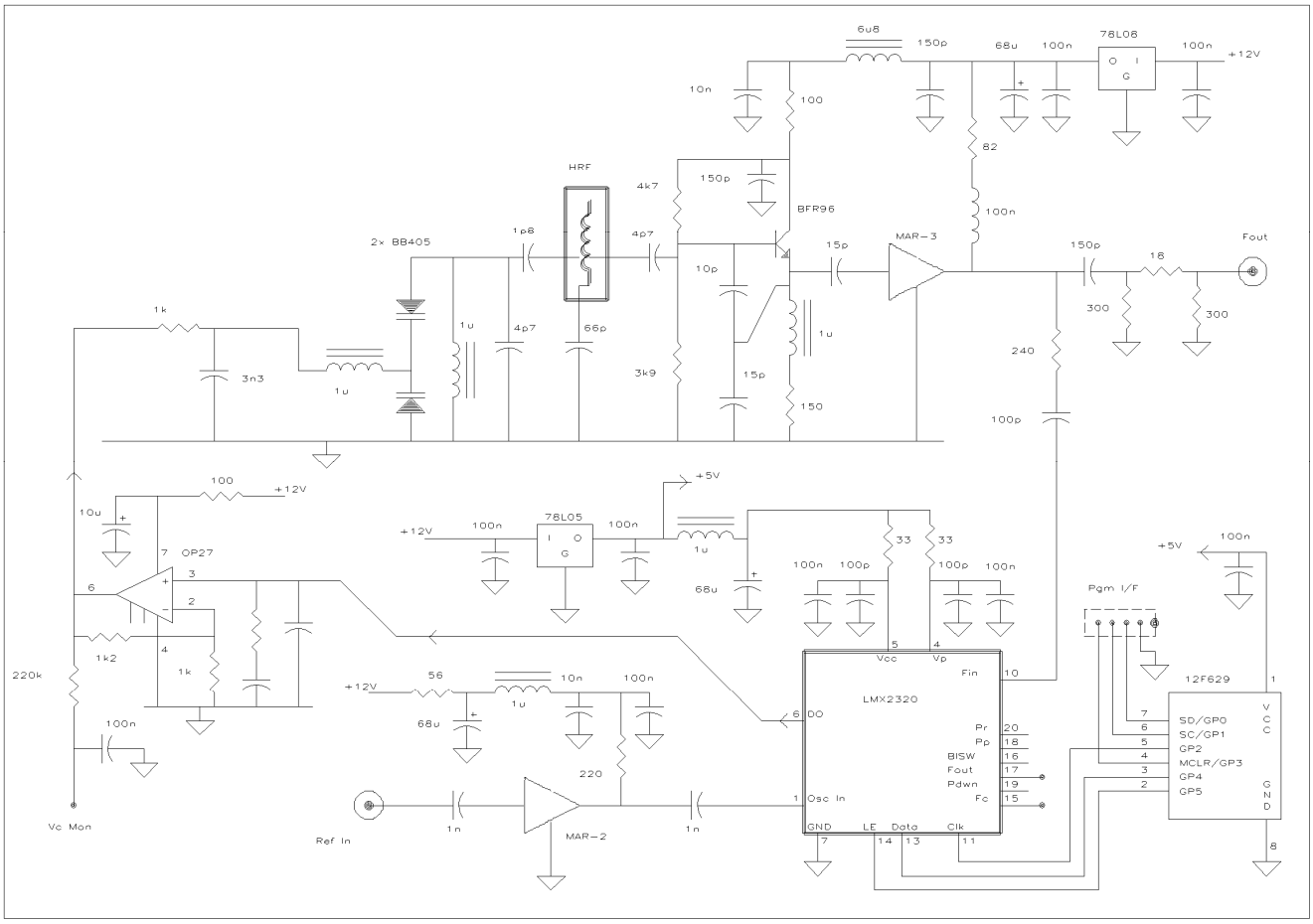


Figure 3 Circuit diagram of final PLL

An opamp buffer was also added to give a wider tuning voltage swing and to stiffen up the drive to the varicap, and allow extra filter poles to be added as needed. At the relatively high loop bandwidth – close to the maximum possible, PLL filter components become quite non critical and even a single RC gave a result not dissimilar to the phase noise plot in Figure 4

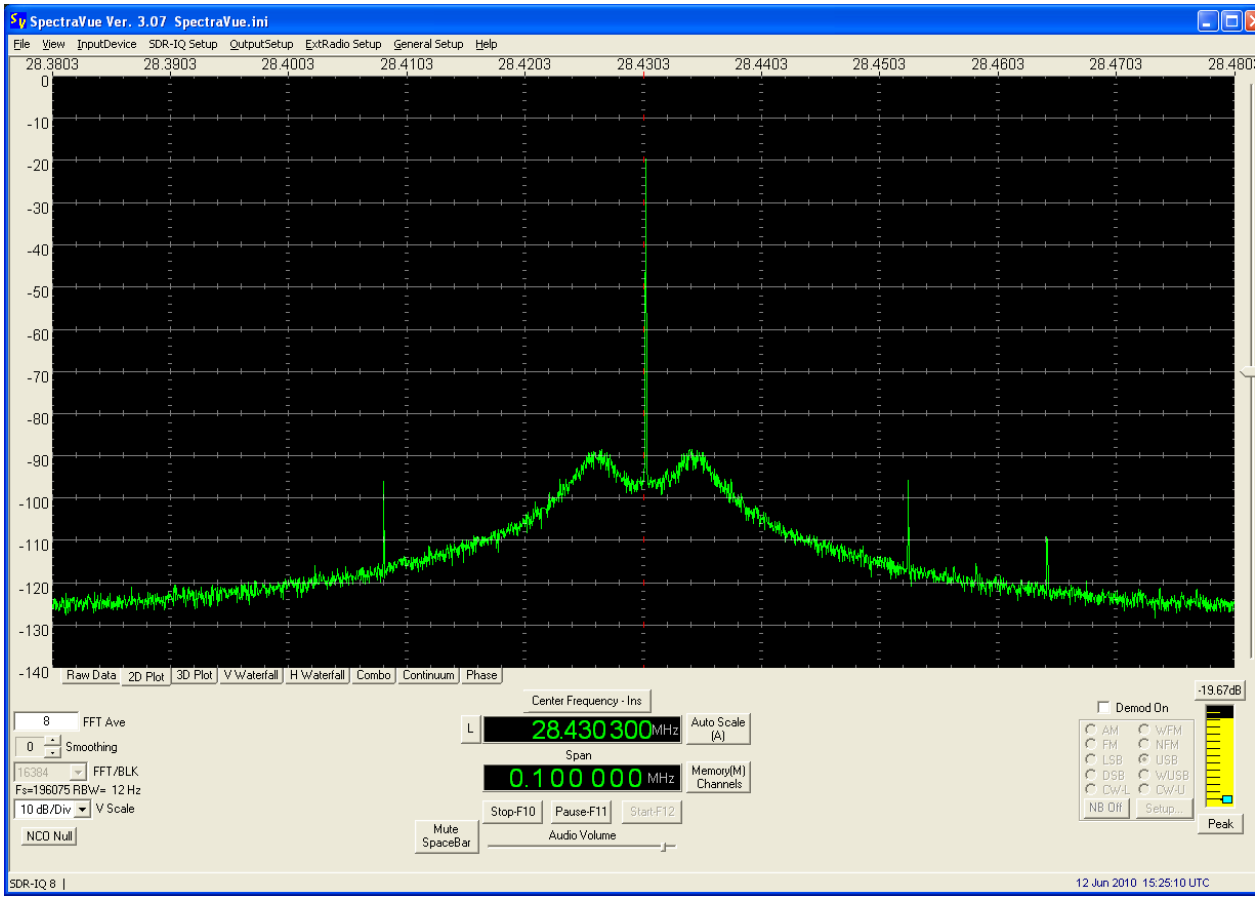


Figure 4 Phase noise plot at Fcomp = 172kHz PLL BW = 16kHz

However, the plot still shows a considerable worsening of the phase noise outside the loop bandwidth compared with that of the free running VCO, so noise from the PLL was still influencing the result.

Intuitively, the loop bandwidth only needs to be sufficient to clean up and stabilise the VCO inside a bandwidth necessary for the final listener. Here we are interested in an SSB bandwidth and the ear, so a 3kHz bandwidth ought to be sufficient.

Keeping the same 172kHz Fcomp, the PLL filter values were recalculated for a 6kHz loop bandwidth. The resulting phase noise plot is appreciably improved as can be seen in Figure 5 The spurious lines seen come from the DDS. Reference frequency sidebands at +/-172kHz are less than -90dBc.

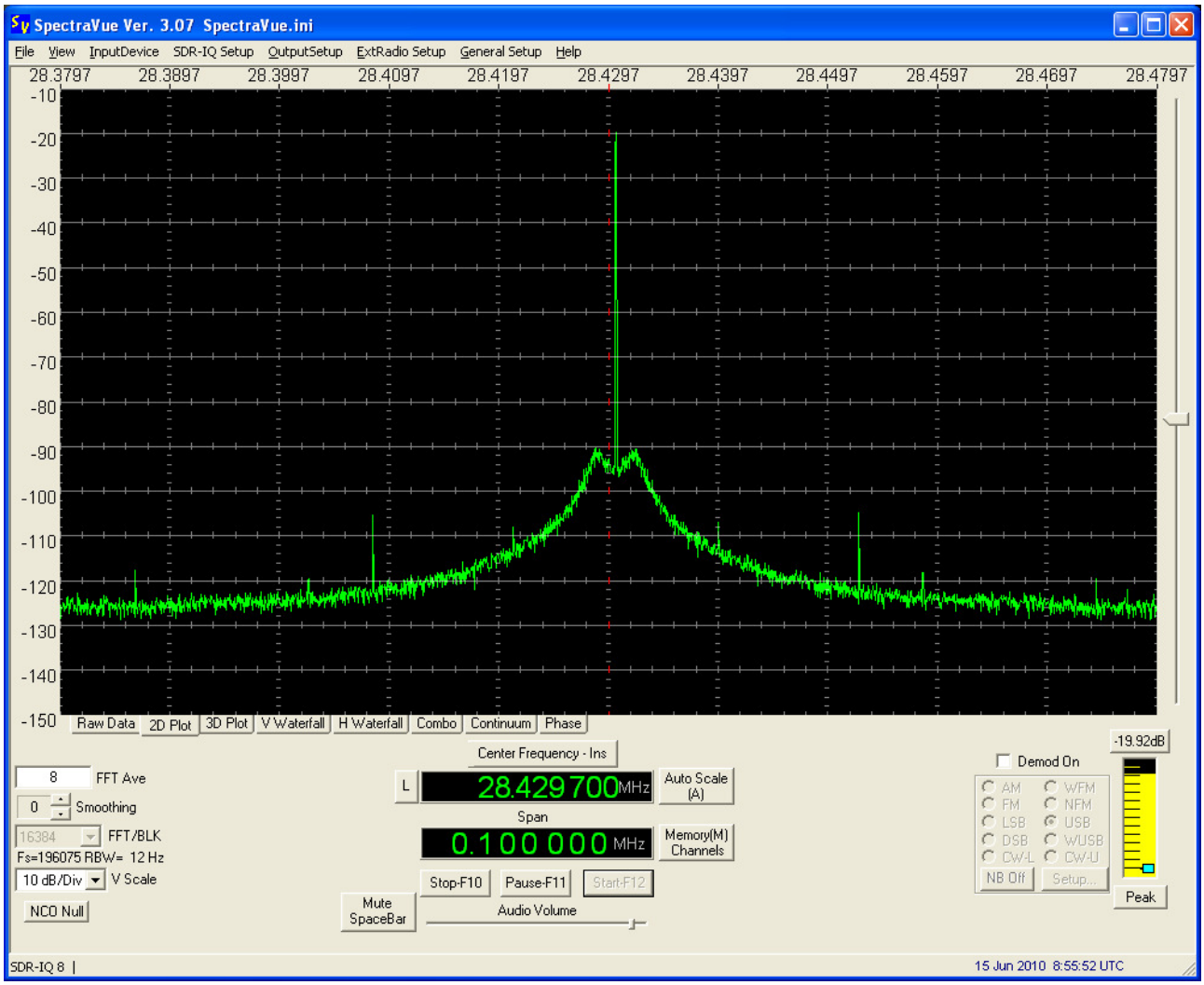


Figure 5 Phase noise plot at Fcomp = 172kHz PLL BW = 6kHz

It can be seen that inside the loop bandwidth, and that detectable in a standard SSB bandwidth phase noise is of the order of -85dBc/Hz, which in 3kHz means that background noise would be 50dB below the carrier tone. At 20kHz spacing the level is around -115dBc/Hz. A result is more than likely acceptable to all.

On Air Tests

With the DDS programmed to generate a JT65B and FSK CW sequence the beacon was put on air, radiating around 1 Watt EIRP from crossed dipoles. Figure 6 shows the spectrum during the JT65B sequence.

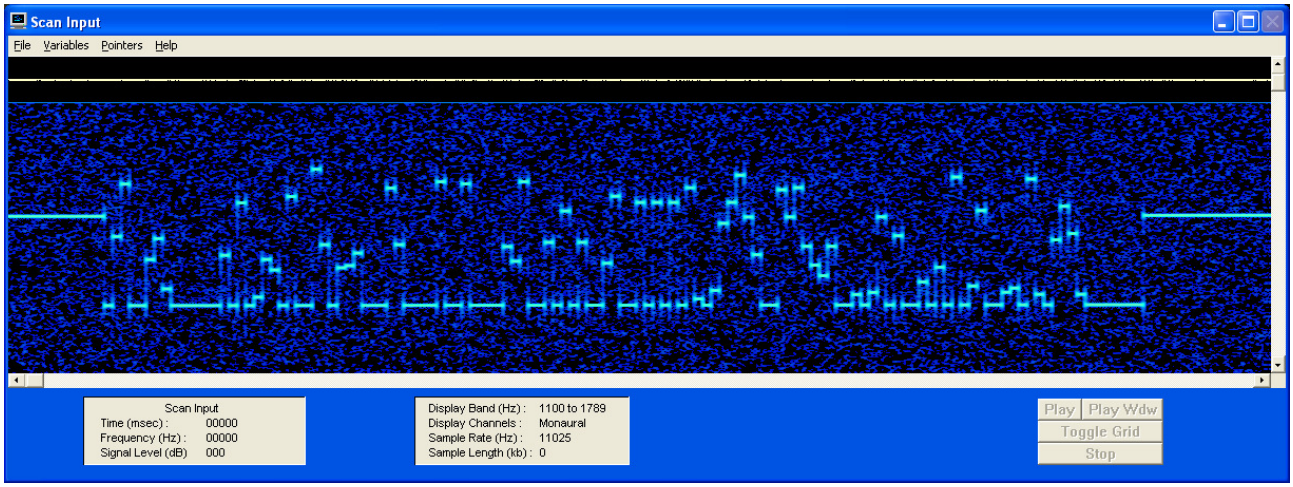


Figure 6 Beacon transmitter spectrum while sending the JT65B sequence

[1] www.g4jnt.com/432_Beacon_Source_First_Tests.pdf